Slide 1

Administrivia

- Homeworks 6 and 7 graded. I will mail averages so far and approximate letter grades later today.
- Solutions to all quizzes on Web.
- Review sheet on Web.
- Review session 3pm Monday. (Okay?)
- Extra-credit problems still in work. Will be on Web by Monday. Due following Monday. *Can only help your grade.* (Maximum of 30 points, which would increase your average by about 5 points.)

Slide 2

A Little More About Memory Hierarchies

- Standard picture shows registers, cache, main memory, disk.
- "Cache" can really be several levels, each faster and more expensive than the one below. Level one (L1) cache usually on chip with processor, other levels not. Generally managed by hardware (as part of "memory management unit" (MMU)). "Set associative" cache is compromise between simplicity of direct mapped cache and flexibility of fully associative cache.

Slide 3

A Little More About Processor Improvements

- "Deeper" pipelines (more stages — 20 or 30 in some recent processors): More potential for speedup but more complicated to build and more potential for the various hazards. Many very sophisticated schemes for keeping pipeline full / not stalled.
- "Superscalar" architecture: Idea is to duplicate some functional units and allow CPU to execute more than on instruction at a time. Requires complicated "dispatch" hardware to determine what instructions can be done in parallel.
- VLIW ("very long instruction word"): Another form of "instruction-level parallelism", but encoded in instructions themselves, so figuring out what can be done in parallel is compiler's job.

Slide 4

A Little More About Processor Improvements, Continued

- "Simultaneous multithreading": Processor executes instructions from different "threads" in parallel. Intel calls their version "hyperthreading". Supposedly allows a single processor to look to the o/s like two logical processors.
- Multi-core chips: Multiple processors on a single chip. May or may not share L1 cache.

Slide 5

Review of Topics

- A little about performance.
- MIPS assembler language.
- Translating C to MIPS assembler language.
- Binary representation of instructions.
- Binary representation of data (integers, ASCII, floating-point numbers).
- Computer arithmetic.
- Gate-level logic design.
- Design of a processor — ALU, datapath, control.
- Other schools spread this material (plus some, okay) over three courses! so, we have done a lot!

Slide 6

Minute Essay

- None — sign in.