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## A Little About make Motivation: Most programming languages allow you to compile programs in pieces ("separate compilation"). This makes sense when working on a large program — when you change something, just recompile parts that are affected. Idea behind make — have computer figure out what needs to be recompiled and issue right commands to recompile it.

Makefiles
• First step in using make is to set up "makefile" describing how files that make up your program (source, object, executable, etc.) depend on each other and how to update the ones that are generated from others. Normally call this file Makefile or makefile.
Simple example (assuming main.c #includes defs.h and foo.h):
main: main.o foo.o gcc -o main main.o foo.o
main.o: main.c defs.h foo.h gcc -c main.c
foo.o: foo.c gcc -c foo.c
• When you type make, make figures out (based on files' timestamps) which files need to be recreated and how to recreate them.

Predefined Implicit Rules
make already knows how to "make" some things — e.g., foo or foo.o from foo.c.
In applying these rules, it makes use of some variables, which you can override.
A simple but useful makefile might just contain: CFLAGS = -Wall -pedantic -0
Or you could use CFLAGS = -Wall -pedantic \$(OPT) OPT = -0 and then optionally override the -O by saying, e.g., make OPT=-g foo.

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