

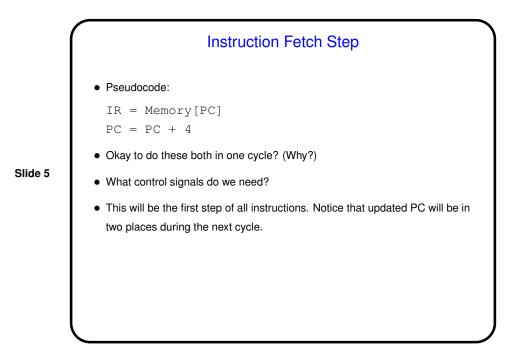
## Datapath for Multiple-Cycle Implementation, Continued

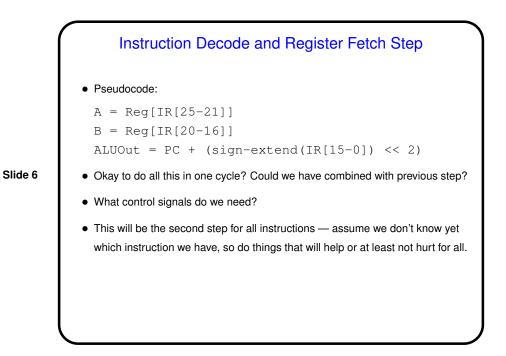
• Is this okay? For R-format instructions and load/store word, yes. For j and beq, we need some more stuff — figure 5.33.

Meanings of control signals in figure 5.34.

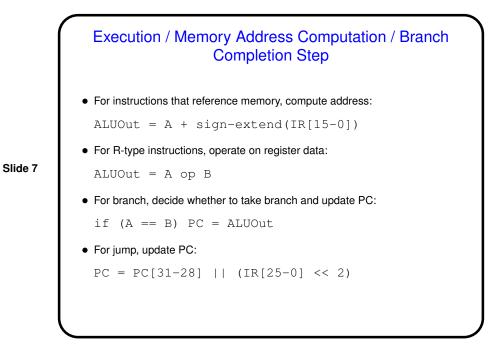
- Notice that most *but not all* of the "temporary storage" areas change every step. What's the exception, and why?
- Next step define "steps" for instructions.



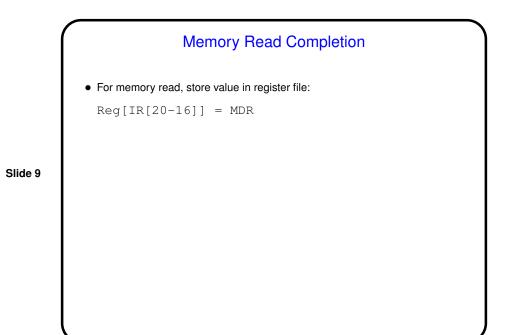


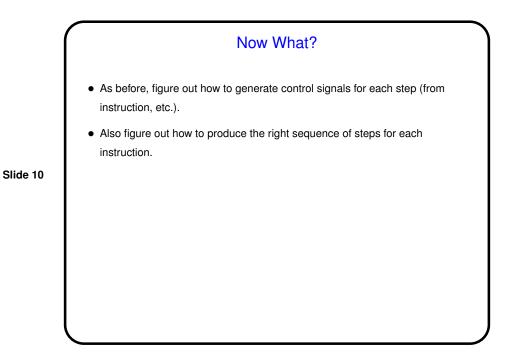


Slide 8



Memory Access / R-Type Instruction Completion
. For memory-access instructions, read/write memory:
 MDR = Memory[ALUOut]
 or
 Memory[ALUOut] = B
. For R-type instruction, store result into register:
 Reg[IR[15-11]] = ALUOut





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Looking at figure 5.33, what control signals do we need for the "instruction fetch" step? Give values for all of the following (or as many things on the figure as you have time to decide about):		
RegDst	RegWrite	ALUSrcA
MemRead	MemWrite	MemtoReg
IorD	IRWrite	PCWrite
PCWriteCond	ALUSrcB	PCSrc
Pseudocode, again:		
IR = Memory[PO	C]	
PC = PC + 4		