## Administrivia

- Reminder: Homework 6 due Wednesday.


## Slide 1

## Generating Control Signals

- For single-cycle implementation, we could write down a truth table, claim we could turn that into a CL block, and be done. (How did we get from one "step" to the next?)
- For multi-cycle implementation, it will be more interesting. Look at two ideas:

Slide 2 "finite state machines" and "microprogramming".

## Finite State Machines

- Definition:
- Set of states, inputs, outputs.
- Next-state function mapping inputs and current state to next state.
- Output function mapping inputs and current state to outputs. (For "Moore


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 machines", which we'll use, output depends only on current state.)- Typically represented pictorially, showing outputs of each state and how inputs cause transitions from one state to another. Probably clearest from an example...


## Finite State Machines, Example

- Example from appendix B - simplified traffic signal for intersection of $N / S$ and E/W streets:
- Inputs are sensors indicating whether cars are waiting, one for each direction ( $\mathrm{N} / \mathrm{S}$ or $\mathrm{E} / \mathrm{W}$ ).

Slide $4 \quad$ - Outputs are two signals, "green in N/S direction" and "green in E/W direction".

- Two states corresponding to two outputs.
- Can first develop the idea pictorially, then write down in table form. Details in appendix B (B.6).
- Sketch of required hardware - figure B.29.


## Generating Control Signals with a FSM

- For this approach to generating control signals, we'll design a finite state machine such that:
- States represent moving through the five steps we outlined.
- Outputs are control signals (as previously defined).


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- In representing this pictorially, we'll simplify a little:
- Input to multiplexors we "care about" will be given (0/1, 00/01/10/11, etc.)
- Other control signals will be listed if 1 , not listed if 0 .
- High-level view in figure 5.36 , details in subsequent figures, with figure 5.42 showing the whole thing.


## Generating Control Signals with a FSM, Continued

- So our idea is to have something like figure B.29, such that:
- Inputs are 6 bits of opcode (since we'll decide what state is next based on current state and opcode).
- State is 4 bits (contained in a 4-bit register). (Why 4 bits?)

Slide $6 \quad$ - Outputs are control signals.

- This then replaces "control" in figure 5.33.


## Minute Essay

- Sketch a finite state machine for a slightly improved traffic signal:
- Inputs are sensors as described plus a "flash both directions" input.
- Outputs are "N/S green" and "E/W green" as described, plus "N/S flash" and "E/W flash".

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- Operation should be as before, except that whenever the "flash both directions" input is on, the two "flash" outputs should be 1 and the two "green" outputs should be 0 .

