

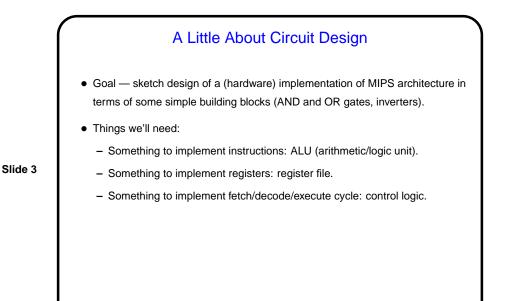
Floating Point in MIPS Architecture
Architecture defines 32 floating-point registers (\$f0 through \$f31), used singly for single-precision, in pairs for double-precision.
Instruction set includes:

Arithmetic instructions:
add.s, sub.s, mul.s, div.s; add.d, sub.d, mul.d, div.d
Load/store instructions (single-precision):
lwc1; swc1

Comparisons:

c.eq.s, c.lt.s, etc.; c.eq.d, c.lt.d, etc.
These set a bit true/false, which can be used by bclt, bclf.

Slide 2



## Implementing Logic Gates — Executive-Level Summary

- The ones and zeros of low-level software become two distinct voltages in hardware, and the logic of Boolean algebra is implemented using "switches" (things that connect an input to an output, or not, depending on the state of a control input).
- Slide 4
- Currently these switches are (usually?) transistors. In widely-used "CMOS technology", there are two types of switches, one that's good if the input is "one" and one that's good if the input is "zero". These can be combined to implement logic. Simple example: Inverter. (See link from "useful links" page.)

