Slide 1

## Administrivia

- Reminder: Homework 4 due (if you didn't turn in Friday).

Slide 2

## SRAM and DRAM

- What about RAM (Random Access Memory)? in some ways, extension of register-file idea — Figure C.9.1.
- Internal details are different, though, and there are two options:
  - Static RAM ("SRAM"), which maintains state as long as there's power.
  - Dynamic RAM ("DRAM"), which has to be refreshed periodically.

  (Guess which one "costs" more.)

Slide 3

## The Big Picture, Revisited

- We've sketched what we need for the "datapath" part of a MIPS processor — combinational logic blocks to perform arithmetic/logic operations (ALU) and store information (register file).
- Now we need something to control it — a sequential logic block.

Slide 4

## Finite State Machines

- Typically represent sequential logic blocks as "finite state machines", consisting of
  - Input(s).
  - Output(s).
  - Current state (one of a set of possible states).
- Define FSM by Boolean expressions that map
  - Current state and input(s) to next state.
  - Current state and (optionally) input(s) to output(s).
- Appendix C example — controlling a traffic light. (Figures C.10.1 through C.10.3 and surrounding text.)

**Slide 5**

## Minute Essay

- Is this material from Appendix C making sense to you? any questions before we move on?
- Would you object if we only have 5 quizzes, not 6? I would still drop the low score.