

Slide 1

Slide 2











Slide 6



Floating Point in MIPS Architecture
Architecture defines 32 floating-point registers (\$f0 through \$f31), used singly for single-precision, in pairs for double-precision.
Instruction set includes:

Arithmetic instructions:
add.s, sub.s, mul.s, div.s; add.d, sub.d, mul.d, div.d
Load/store instructions (single-precision):
lwcl; swcl

Comparisons:

c.eq.s, c.lt.s, etc.; c.eq.d, c.lt.d, etc.
These set a bit true/false, which can be used by bclt, bclf.

Slide 7

Slide 8



