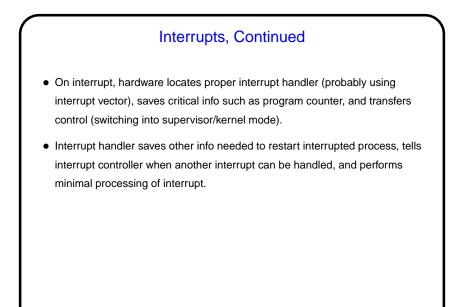


Interrupts, Continued
I/O device "interrupts" by signalling interrupt controller.
Interrupt controller signals CPU, with indication of which device caused interrupt, or ignores interrupt (so device controller keeps trying) if interrupt can't be processed right now.
Processing is then similar to what happens on traps (interrupts generated by system calls, page faults, other errors) ...



## Interrupts, Continued

- Worth noting that pipelining (very common in current processors) complicates interrupt handling when an interrupt happens, there could be multiple instructions in various stages of execution. What to do?
- "Precise interrupts" are those that happen logically between instructions. Can try to build hardware so that this happens always, or sometimes.
- "Imprecise interrupts" are the other kind. Hardware that generates these may provide some way for software to find out status of instructions that are partially complete. Tanenbaum says this complicates o/s writers' jobs.

