









Mechanisms for Swapping
In a sense, managing swapping is much like managing TLB misses, though unlike with those it always involves the O/S:
Page-table entry also has bit indicating that page is valid but not present in memory. (Could combine with bit that says "not valid".)
In translating a virtual address, MMU still first tries TLB; on a miss, translates using page table. If page valid but not present, generates a "page fault" interrupt, transfers to O/S's handler for those.
(Recall that TLB misses can be handled in hardware or software. Simpler to understand if done by hardware, but principles the same.)

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