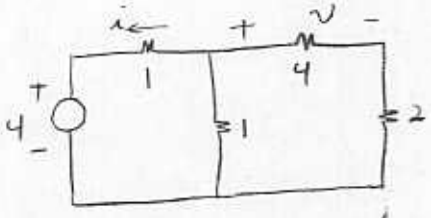
# ENGR. 2364
## Handout #1
## Review of KCL and KVL

(1) Consider the circuit shown below. Find $i$ and $v$.



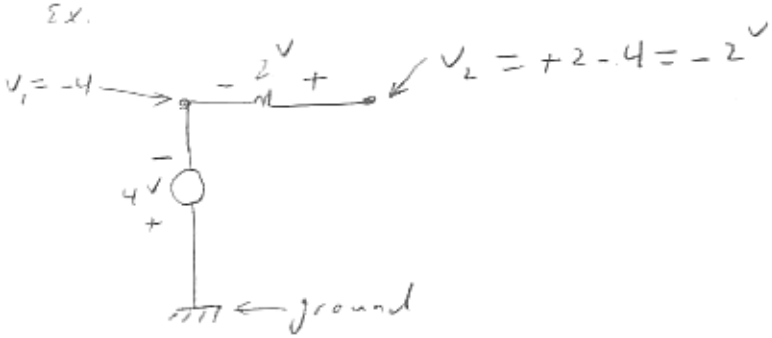

First, let's apply nodal equations or KCL to this problem.

KCL in a nutshell

(a) choose a reference node also called 0V reference node or ground

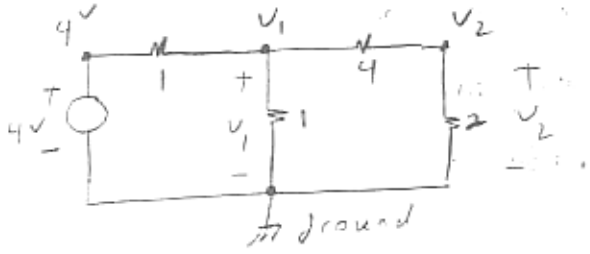
(b) The voltage at every other node with respect to the reference node is the algebraic sum of all the voltages you observe when you move from that node to ground. Algebraic sum means that as you pass through an element, for voltage drop you pick up the first sign you see.

Ex.



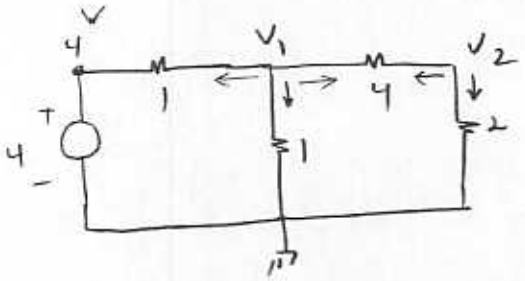

(c) you label unknown node voltages with $v_1, v_2, \ldots v_n$ and try to find them by writing KCL at different nodes.

Now, Let's do the problem stated above using KCL.




Note that in KCL, the voltage label at every node is really the voltage at that node with respect to ground with that node taking

the positive sign of the voltage drop and ground being negative.



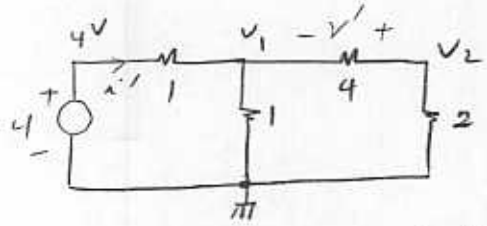

Note: Do not write KCL at the node connected to the 4V power supply.

$$\begin{cases} \dfrac{V_1-4}{1}+\dfrac{V_1}{1}+\dfrac{V_1-V_2}{4}=0 \\ \dfrac{V_2-V_1}{4}+\dfrac{V_2}{2}=0 \end{cases} \Rightarrow V_1=\frac{8}{13}\text{V},\ V_2=\frac{8}{39}\text{V}$$

Now, we can find the information of interest.

$$i=\frac{V_1-4}{1}=\frac{8}{13}-4=\frac{-44}{13},\quad V=V_1-V_2=\frac{16}{39}$$

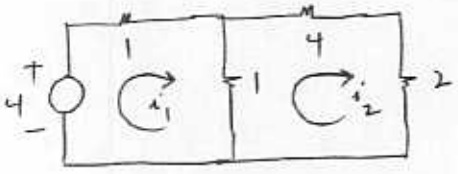
Now, what if you need to find $i'$ and $v'$ shown below.




$$i'=\frac{4-V_1}{1}=\frac{44}{13}$$

$$v'=V_2-V_1=-\frac{16}{39}$$

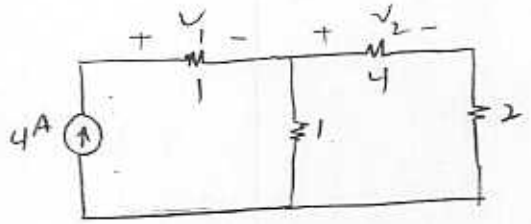
Next, let's solve the same problem using KVL.



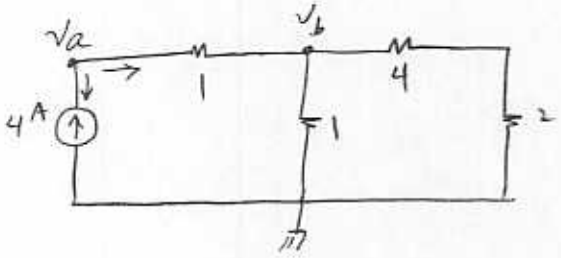

$$\begin{cases} -4+i_1'+1(i_1'-i_2')=0 \\ 1(i_2'-i_1')+4i_2'+2i_2'=0 \end{cases}$$ solve for $i_1'$ and $i_2'$.

Then $i=-i_1'$ and $v=4i_2'$.

(2) Consider the circuit shown below. Find $v_1$ and $v_2$.




First, we write KCL.

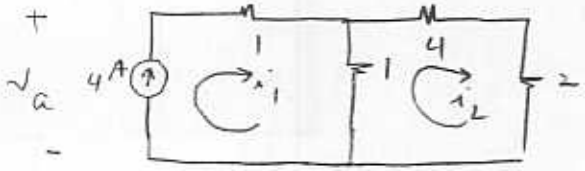



$$\begin{cases} -4 + \dfrac{v_a - v_b}{1} = 0 \\ \dfrac{v_b - v_a}{1} + \dfrac{v_b}{1} + \dfrac{v_b}{6} = 0 \end{cases}$$ solve for $v_a$ and $v_b$.

Then $v_1 = v_a - v_b$

$v_2 = \dfrac{v_b}{6} \cdot 4$ This is voltage division

Next, we write KVL.



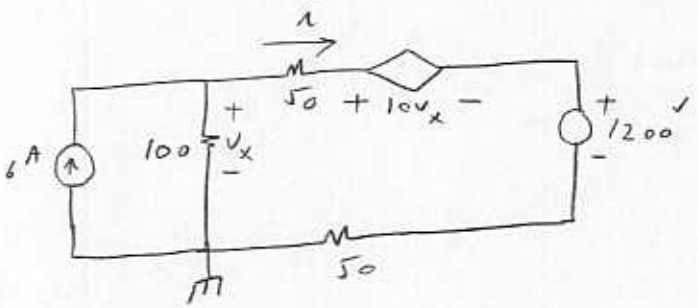

$i_1 = 4$

① $-v_a + 1i_1 + 1(i_1 - i_2) = 0$

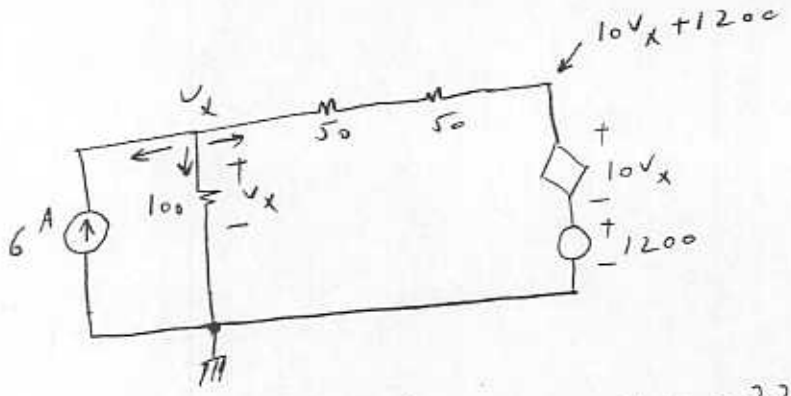
② $1(i_2 - i_1) + 4i_2 + 2i_2 = 0$ ⇒ Solve for $i_2$. Then from eq. ①, solve for $v_a$.

Then $v_1 = 1i_1 = 4$ V, $v_2 = 4i_2$

(3) Find $v_x$ and $i$.



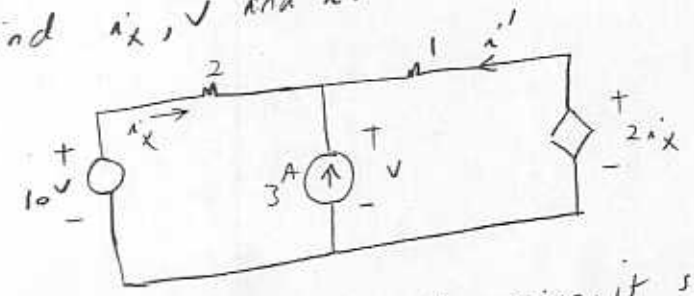

First, Let's redraw the circuit to see things better.



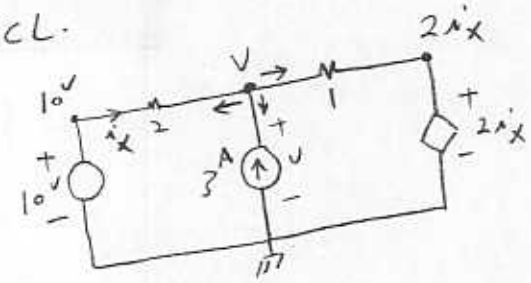

$$-6 + \frac{V_x}{100} + \frac{V_x - (10V_x + 1200)}{100} = 0 \Rightarrow V_x = -225^{V}$$

$$i = \frac{V_x - (10V_x + 1200)}{100} = -32.25^{A}$$

(4) Find $i_x$, V and $i'$




First, Let's redraw the circuit showing information important in KCL.



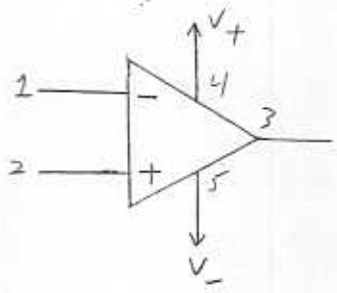

$$\frac{V-10}{2} - 3 + \frac{V - 2i_x}{1} = 0$$

also note that $i_x = \frac{10 - V}{2}$.

solve For $i_x$ and V.

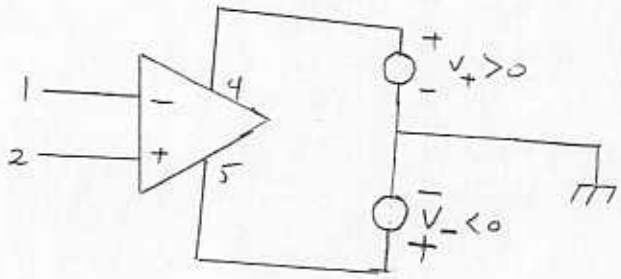
Then $i' = \frac{2i_x - V}{1}$.

# ENGR. 364
## Handout #2
## Ideal Operational Amplifiers

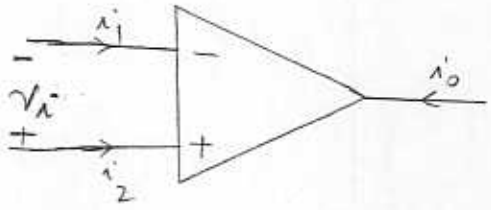



1: inverting input
2: non-inverting input
3: output
4: positive DC power supply
5: negative DC power supply

An op amp does not have a ground pin. Ground is external and where the two supplies meet.




An ideal op amp has the Following properties:

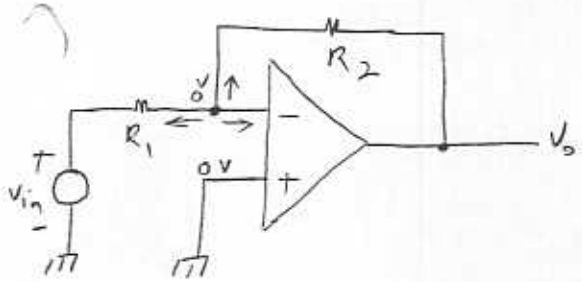



$$\begin{cases} i_1 = 0 \\ i_2 = 0 \\ v_i = 0 \end{cases}$$

These three properties are enough to analyse ideal op amp circuits

Note that $i_o$ is not zero. Its value is not known initially. This is why you must avoid writing KCL at the output of an op amp at the beginning. IF you are required to Find $i_o$, you can Find it at the end by writing KCL at the output node

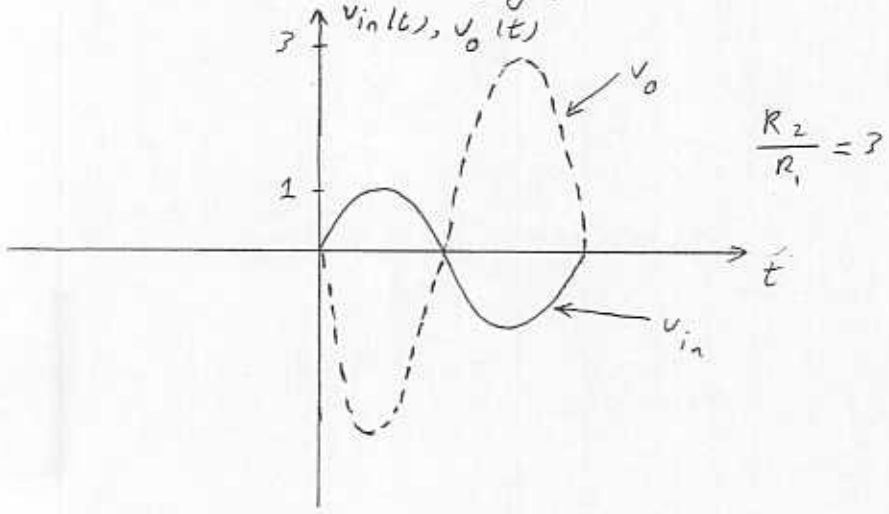
Ex. 1: Inverting amplifier:




$KCL \Rightarrow \frac{0-V_{in}}{R_1} + 0 + \frac{0-V_o}{R_2} = 0 \Rightarrow V_o = -\frac{R_2}{R_1} V_{in}$

if $\frac{R_2}{R_1} > 1 \Rightarrow$ we have an amplifier because $\left|\frac{V_o}{V_{in}}\right| > 1$.

This amplifier is inverting because $V_{in}$ and $V_o$ are always out of phase because of the minus sign.




IF $V_{in} = 1^V \Rightarrow$ For $\frac{R_2}{R_1} = 5$, we have $V_o = -5^V$

IF $V_{in} = 1^V \Rightarrow$ For $\frac{R_2}{R_1} = 10$, we have $V_o = -10^V$

IF $V_{in} = 1^V \Rightarrow$ for $\frac{R_2}{R_1} = 15$, we have $V_o = -15^V$

IF $V_{in} = 1^V \Rightarrow$ for $\frac{R_2}{R_1} = 20$, we have $V_o = -20^V$ ✗ No!

IF $V_{in} = 1^V \Rightarrow$ for $\frac{R_2}{R_1} = 100$, we have $V_o = -100^V$ ✗ No!

Note that for an op amp, $V_o$ is limited by the power supplies $V_-$ and $V_+$.

$$V_- \leq V_o \leq V_+$$

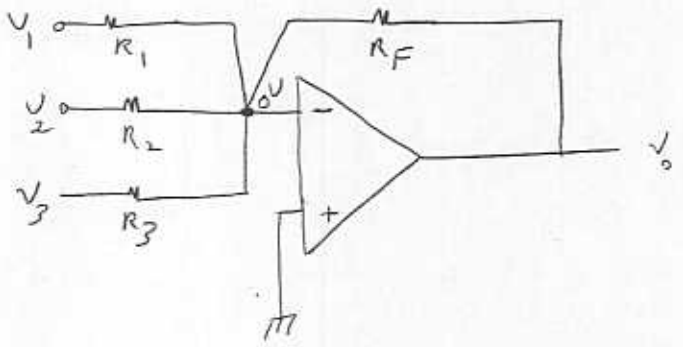
IF $V_- = -15^V$ and $V_+ = 15^V$ (typical values), then the allowed range of $V_o$ is given by $-15^V \leq V_o \leq 15^V$.

IF $V_{in} = 1^V \Rightarrow$ For $\frac{R_2}{R_1} = 20$, we have $V_o = -15^V = V_-$

IF $V_{in} = 1^V \Rightarrow$ For $\frac{R_2}{R_1} = 100$, we have $V_o = -15^V = V_-$

For these two cases, we say the op amp is saturated because it can not follow the output $V_o = -\frac{R_2}{R_1} V_{in}$ any more.

EX. Summer:

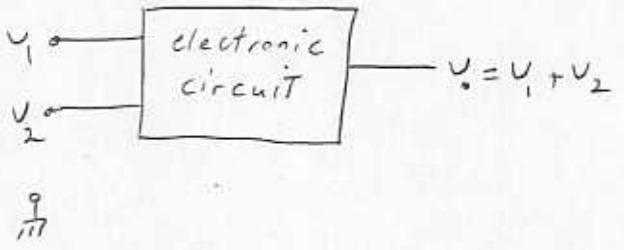


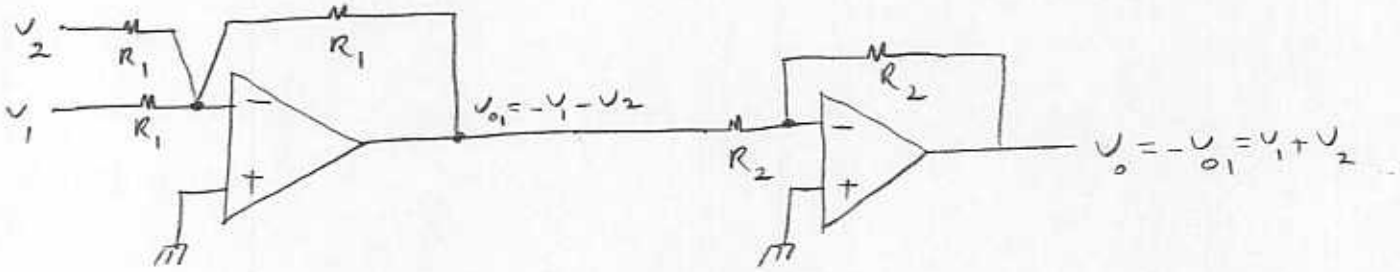

KCL $\Rightarrow \frac{0-V_1}{R_1} + \frac{0-V_2}{R_2} + \frac{0-V_3}{R_3} + 0 + \frac{0-V_o}{R_F} = 0$

$\Rightarrow V_o = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3\right)$

This is a summer. Every input voltage $V_i$ $(i=1,3)$ makes a contribution of $\frac{R_F}{R_i}$ to the output. We can extend this to any number of supplies.

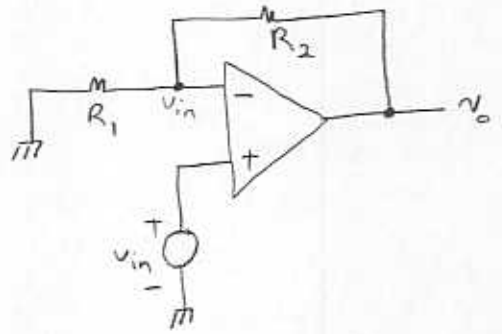
EX. Design an electronic circuit that adds two input voltages.




This is how you add two voltages

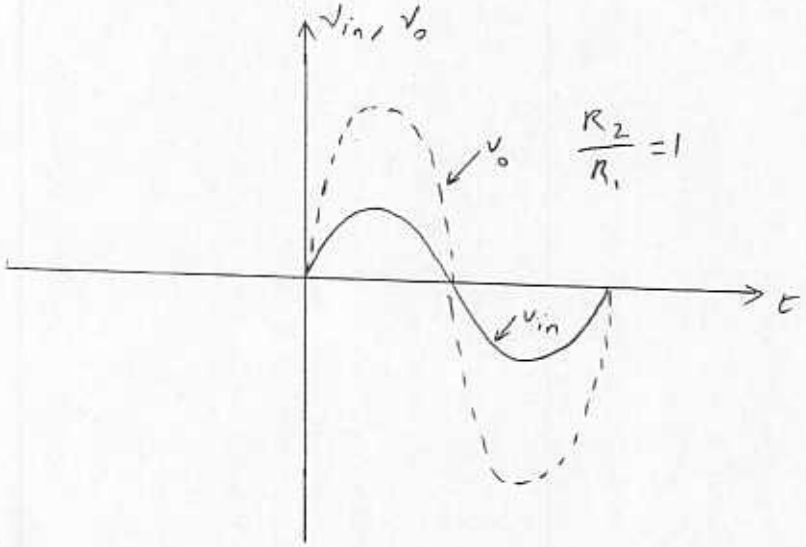
Ex. Non-inverting amplifier:




$$\frac{V_{in}}{R_1} + \frac{V_{in} - V_o}{R_2} - 0 = 0 \Rightarrow V_o = \left(1 + \frac{R_2}{R_1}\right) V_{in}$$

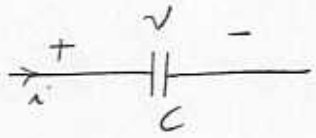
$$\Rightarrow \frac{V_o}{V_{in}} > 1 \Rightarrow \text{This is an amplifier.}$$

Input and output are in phase.



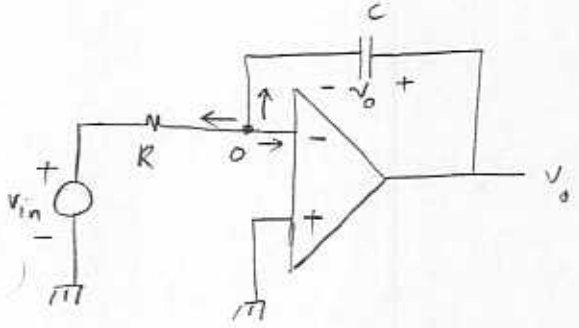

Ex. Integrator

Note that For a capacitor, we have




$$i = C \frac{dV}{dt}$$

Note that $i$ enters through the terminal with positive polarity.




$$\frac{0 - V_{in}}{R} + 0 - C \frac{dV_o}{dt} = 0 \Rightarrow$$

$$\frac{dV_o}{dt} = -\frac{1}{RC} V_{in} \Rightarrow dV_o = -\frac{1}{RC} V_{in}\, dt$$

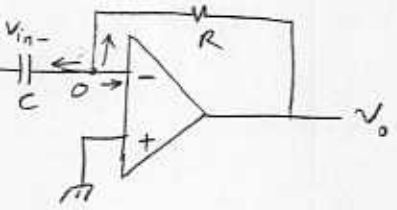
$$\int_{V_o(t=0)}^{V_o(t)} dV_o = -\frac{1}{RC} \int_{t=0}^{t} V_{in}\, dt$$

$$v_o(t) - v_o(t=0) = -\frac{1}{RC}\int_0^t v_{in}\,dt \Rightarrow v_o(t) = v_o(t=0) - \frac{1}{RC}\int_0^t v_{in}\,dt$$

Note that the output $v_o(t)$ is related to the integral of $v_{in}(t)$.

is circuit is called an integrator.

differentiator:

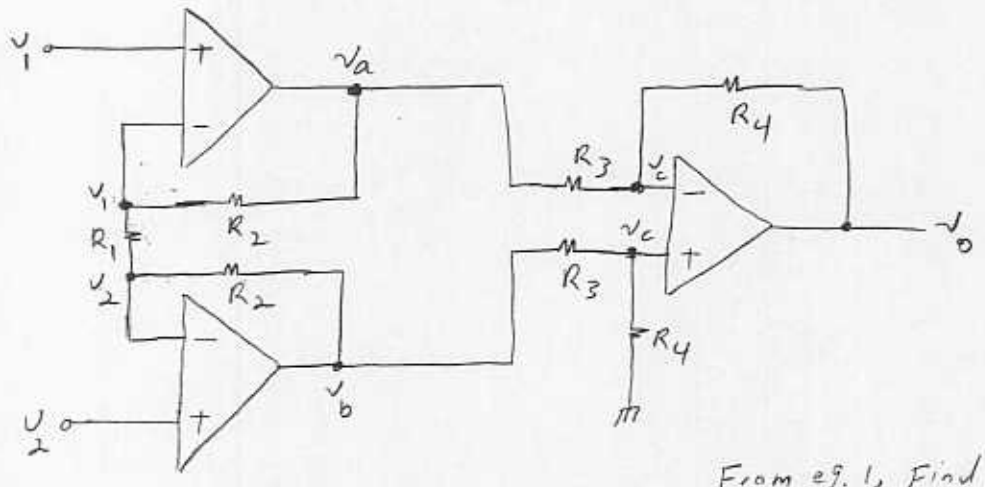



$$-C\frac{dv_{in}}{dt} + \frac{0 - v_o}{R} + 0 = 0 \Rightarrow v_o = -RC\frac{dv_{in}}{dt}$$

Output $v_o$ is the time derivative of the input. This circuit differentiates the input signal with respect to time. This is called a differentiator.

operational amplifier has this name because it can do all sic operations in mathematics. It can add two signals and can integrate or differentiate with respect to time.

ind $v_o$ in terms of $v_1$ and $v_2$:




$$\begin{cases} \text{at } v_1 \Rightarrow 0 + \dfrac{v_1 - v_a}{R_2} + \dfrac{v_1 - v_2}{R_1} = 0 & (1) \\ \text{at } v_2 \Rightarrow \dfrac{v_2 - v_1}{R_1} + \dfrac{v_2 - v_b}{R_2} + 0 = 0 & (2) \\ \text{at } v_c(+) \Rightarrow \dfrac{v_c}{R_4} + \dfrac{v_c - v_b}{R_3} + 0 = 0 & (3) \\ \text{at } v_c(-) \Rightarrow \dfrac{v_c - v_a}{R_3} + \dfrac{v_c - v_o}{R_4} + 0 = 0 & (4) \end{cases}$$

From eq. 1, Find $v_a$ in terms of $v_1$ & $v_2$.
From eq. 2, Find $v_b$ in terms of $v_1$ & $v_2$.
From eq. 3, Find $v_c$ in terms of $v_1$ & $v_2$.
Put all these in eq. 4 to get $v_o$ in terms of $v_1$ and $v_2$.

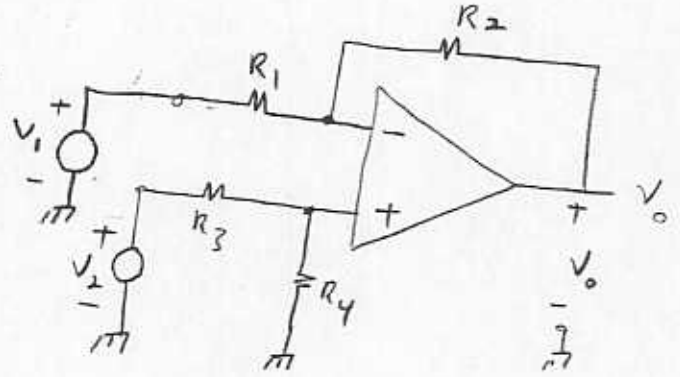
$v_o = (1 + 2R_2/R_1)\,R_4/R_3\,(v_2 - v_1)$

This circuit amplifies the diff. between

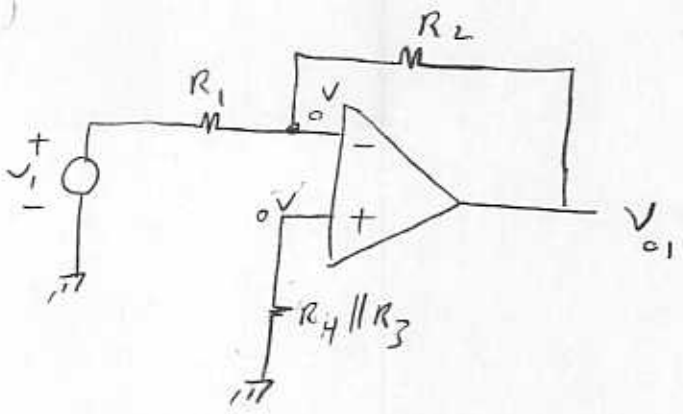
# Supplement to Handout #2

Ex. In the circuit shown below, Find $V_o$ in terms of $V_1$ and $V_2$.

Let's use superposition.
We First consider $V_1$ with $V_2$ shorted out.
We then consider $V_2$ with $V_1$ shorted out.



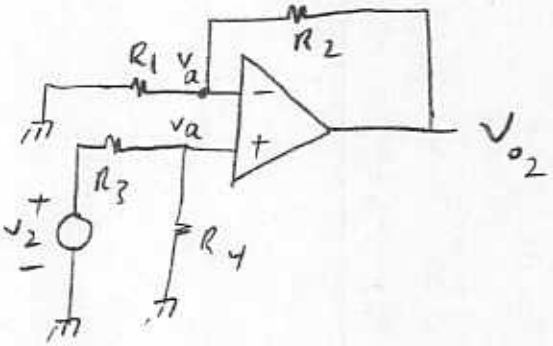

(1) $V_1$ active, $V_2$ shorted out




$$KCL \Rightarrow \frac{0-V_1}{R_1} + \frac{0-V_{o1}}{R_2} = 0 \Rightarrow V_{o1} = -\frac{R_2}{R_1} V_1$$

Inverting configuration

(2) $V_2$ active, $V_1$ shorted out




Series division rule $\Rightarrow$

$$V_a = \frac{R_4}{R_3 + R_4} V_2$$

$$KCL \Rightarrow \frac{V_a}{R_1} + \frac{V_a - V_{o2}}{R_2} = 0 \Rightarrow$$

$$V_{o2} = \left(1 + \frac{R_2}{R_1}\right) V_a = \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} V_2$$

$$V_o = V_{o1} + V_{o2} = -\frac{R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} V_2$$

IF we make $\frac{R_2}{R_1} = \frac{R_4}{R_3}$, $V_o$ reduces to

$$V_o = \frac{R_2}{R_1} (V_2 - V_1).$$

This is a differential amplifier!

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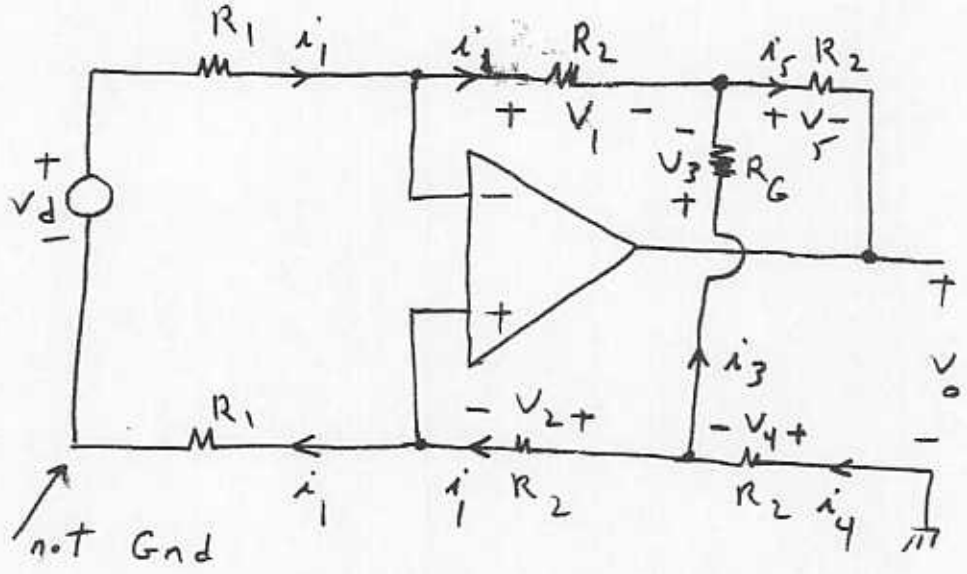
Handout #2
Continued

Prob. 2.

Find $v_o/v_d$.




KVL $\Rightarrow +R_1 i_1' - v_d + R_1 i_1' = 0 \Rightarrow i_1' = v_d/2R_1$

$$v_1 = v_2 = R_2 i_1' = \frac{R_2}{2R_1} v_d$$

KVL $\Rightarrow \frac{R_2}{2R_1 v_d} - v_3 + \frac{R_2}{2R_1} v_d = 0 \Rightarrow v_3 = \frac{R_2}{R_1} v_d$

$$i_3' = \frac{v_3}{R_G} = \frac{R_2}{R_1 R_G} v_d$$

$$i_4' = i_1' + i_3' = \frac{v_d}{2R_1} + \frac{R_2}{R_1 R_G} v_d \;,\; v_4 = R_2 i_4'$$

$$i_5' = i_1' + i_3' = \frac{v_d}{2R_1} + \frac{R_2}{R_1 R_G} v_d \;,\; v_5 = R_2 i_5'$$

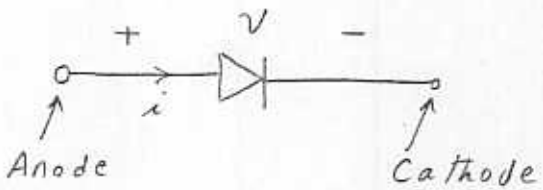
KVL $\Rightarrow -v_o - v_5 - v_3 - v_4 = 0 \Rightarrow v_o = -v_3 - v_4 - v_5 \Rightarrow$

$$v_o = -\frac{2R_2}{R_1}\left[1 + \frac{R_2}{R_G}\right] v_d$$

ENGR.2364
Handout #3

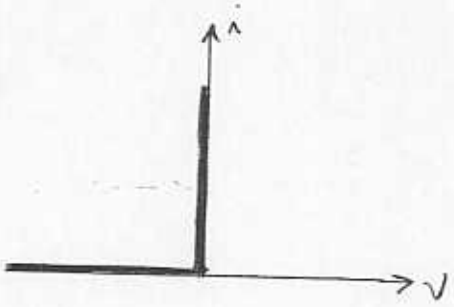
# Diodes

## Ideal diode:

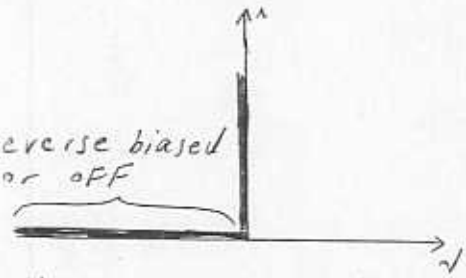



note that the conventional polarity on voltage requires anode to take the plus sign and cathode the minus sign. The conventional current always flow from anode to cathode. You always need to use these conventions.

With the conventional v and i shown above, the i–v characteristic curve of a diode is shown below.

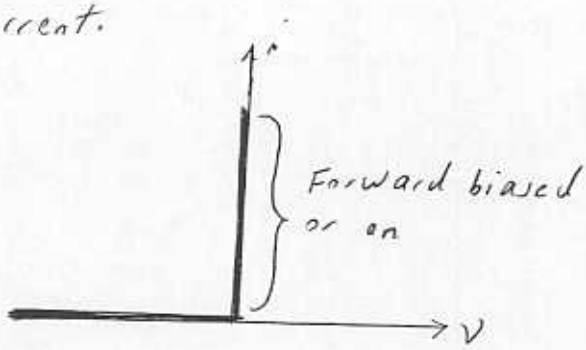



① when $v<0 \Rightarrow i=0$. An ideal diode does not conduct or acts as an open-circuit ($i=0$) when the conventional voltage across it is negative. This region ($v<0$) is called reverse biased or OFF region.




② when $v=0 \Rightarrow i>0$. An ideal diode conducts when $v=0$. Note that when $v=0$, i can take any positive value. The value i takes is determined by the circuit that employs the diode. This region identified by $v=0$ and any value of $i>0$ is called the Forward

biased or on region. Note that in this region the diode acts like a short-circuit because it has zero volts across it and can carry any amount of current.



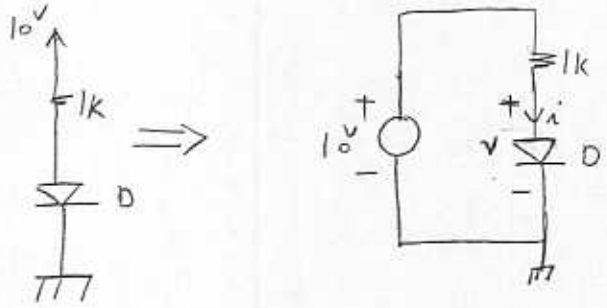

Models of an ideal diode:

① when a diode is off, it has $v<0$ and acts like an open-circuit.
② when a diode is on, it has $i>0$ and acts like a short-circuit.

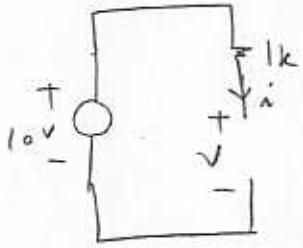
A diode can have two states: on or off. At the begining when we want to solve a problem that has a diode in it, we do not know if the diode is on or off. We make an assumption.

IF we assume the diode is on, we replace it by a short-circuit. We then verify our assumption by finding $i$. IF $i>0$, we have verified our assumption and the diode is truely on. IF $i$ turns out to be less than zero, it means we have made the wrong assumption.
IF we assume the diode is off, we replace it by an open-circuit we then verify our assumption by finding $v$. IF $v<0$, we have verified our assumption and the diode is truely off. IF $v$ turns out to be greater than zero, it means we have made the wrong assumption.
It is very desirable to make the right assumption about the state of a diode because it saves you time. However, if you make the wrong assumption, you will not be able to verify it. You then know that your assumption is wrong and can change it.

Ex.1: Find the voltage across and the current through the diode.

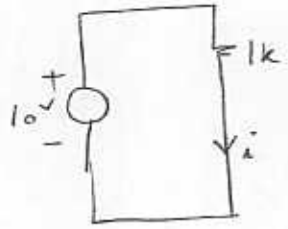



Assume D is OFF

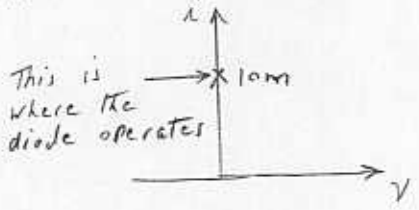



KVL $\Rightarrow -10 + 1k(0) + V = 0 \Rightarrow V = 10^V$ is $V < 0$? No. $\Rightarrow$ D can not be OFF.

Assume D is on.

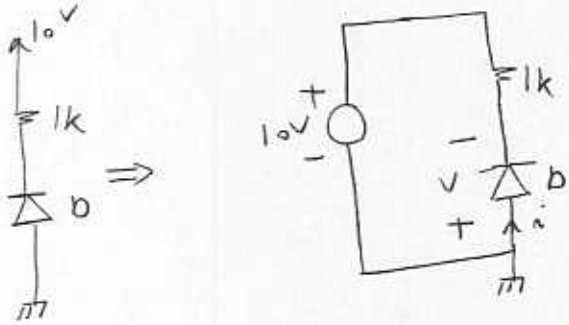



KVL $\Rightarrow -10 + 1k i = 0 \Rightarrow i = \frac{10}{1k} = 10mA$ is $i > 0$? Yes $\Rightarrow$ D is on.

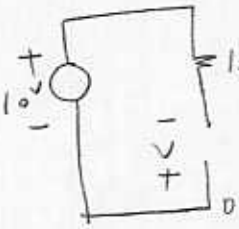



Therefore, D is on, $V = 0$ and $i = 10mA$.

Ex.2. Repeat example 1 For the circuit shown below.



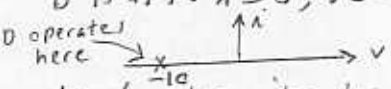

Assume D is OFF $\Rightarrow$




KVL $\Rightarrow -10 + 1k(0) - V = 0$

$\Rightarrow V = -10 < 0$ ✓

D is OFF. $i = 0$, $V = -10^V$.




Note that if a circuit has two diodes, each diode by itself can be on or OFF. There are the following four possibilities For the assumptions you can make.

| diode 1 | diode 2 |
|---|---|
| on | on |
| on | oFF |
| oFF | on |
| oFF | oFF |

Only one combination of diode 1 and diode 2 can be valid in a circuit. Guessing the right assumption takes a lot of practice. With 3 diodes, we have

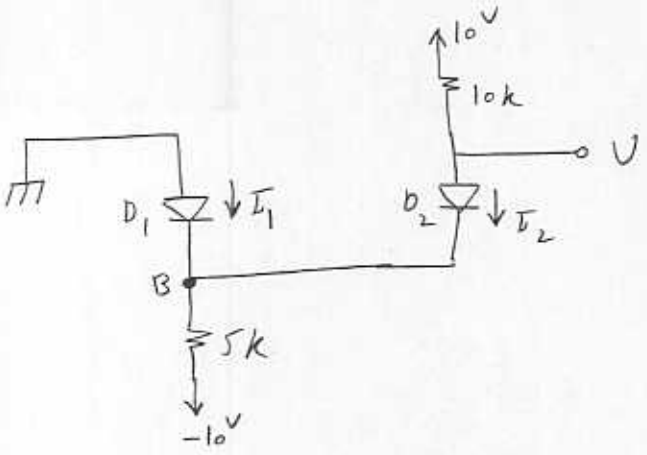
number of diodes → 3

$2 = 8$ possible states

↑ possible states

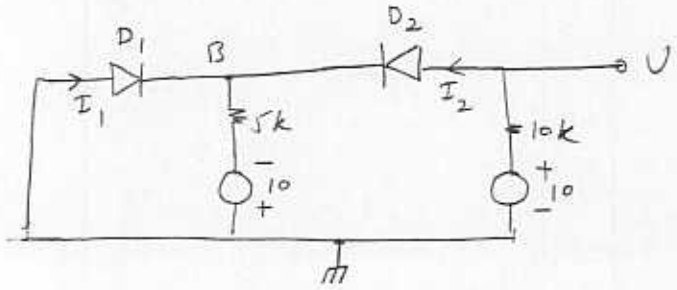
again only one combination of $D_1$, $D_2$ and $D_3$ being on or oFF can holds. You have to guess the right one.

Ex.

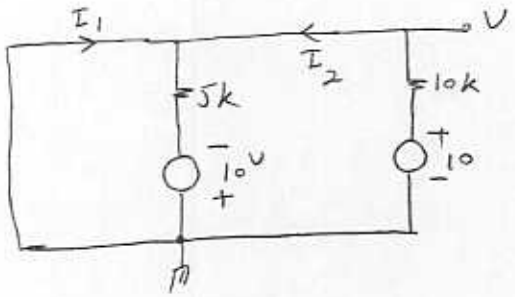



Find $I_1$, $I_2$ and $V$.

Solution: First, redraw the circuit showing all the power supplies.



Assume both diodes are on.



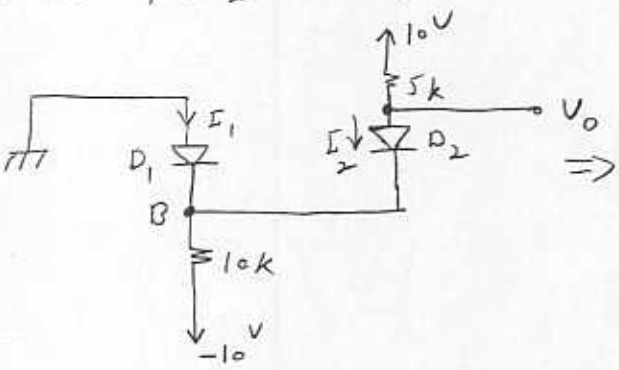

KVL $\Rightarrow -10 + 10k\,I_2 = 0 \Rightarrow I_2 = 1mA > 0$ ✓

KVL $\Rightarrow 5k(I_1 + I_2) - 10 = 0 \Rightarrow I_1 = 1mA > 0$ ✓

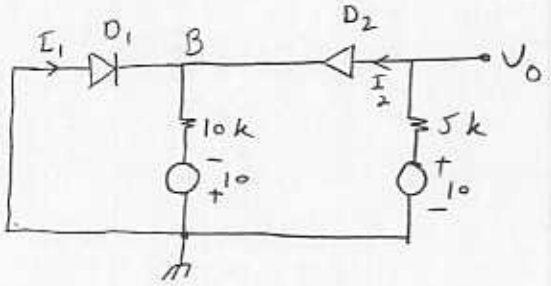
both diodes are on.

KVL $\Rightarrow -V = 0 \Rightarrow V = 0$

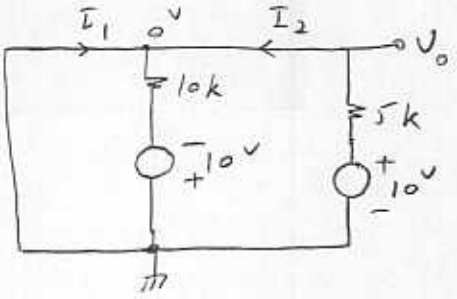
Ex. Find $I_1$, $I_2$ and $V_0$




$\Rightarrow$




Again, let's assume both diodes are on.



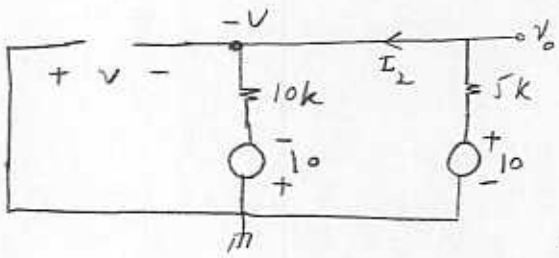

KCL $\Rightarrow -I_1 + \frac{0-(-10)}{10k} + \frac{0-10}{5k} = 0 \Rightarrow$

$I_1 = -1mA$

KVL $\Rightarrow -10 + 5k\,I_2 = 0 \Rightarrow I_2 = 2mA$

$I_1 = -1mA < 0$ ✗ both diodes can not be on.

Assume $D_1$ OFF and $D_2$ on.




KCL $\Rightarrow 0 + \frac{-V-(-10)}{10k} + \frac{-V-10}{5k} = 0 \Rightarrow$

$V = \frac{-10}{3} < 0$ ✓

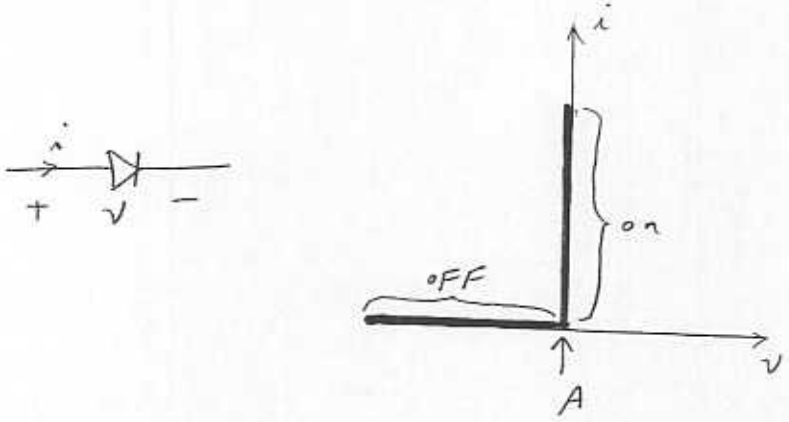
KVL $\Rightarrow -10 + 5k\,I_2 - V = 0 \Rightarrow I_2 = 1.33mA > 0$ ✓

$\Rightarrow D_1$ is OFF and $D_2$ is on.

KVL $\Rightarrow -V_0 - V = 0 \Rightarrow V_0 = -V = \frac{10}{3}V$

$\Rightarrow I_1 = 0,\ I_2 = 1.33mA,\ V_0 = \frac{10}{3}V.$

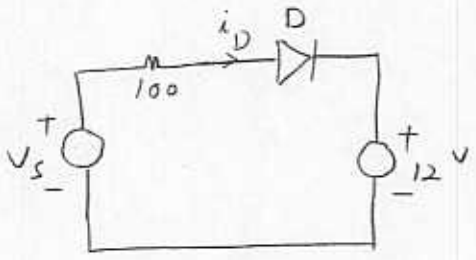
Let's look at the i–v characteristic curve of a diode again.




Point A at which $v=0$ and $i=0$ is the point at which the on and OFF regions meet. If the diode is operating at this point, we say it is operating at the boundary of on and OFF states. By slightly changing the power supplies in the circuit driving this diode, we can make it go into on or OFF states.

Note that up to now, we have only considered DC supplies driving diodes. Since DC supplies never change value in time, diodes do not change states either. They always stay on or OFF. On the other hand, since AC supplies change value with time, a diode driven by these supplies can also change state in time and go from off to on or on to OFF.

Ex. Consider the circuit shown below.

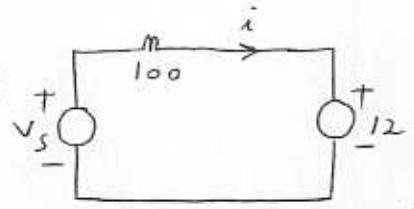



Assume $V_s$ is an AC supply that can take any value in the range $-\infty$ to $+\infty$ in time.

a) plot $i_D \perp V_s$.

b) plot $i_D(t)$ if $V_s(t) = 24\sin t$.

Assume D is on.

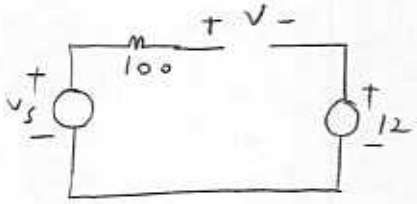



KVL $\Rightarrow -V_s + 100i + 12 = 0 \Rightarrow i = \frac{V_s - 12}{100} > 0$ to verify on.

$\Rightarrow V_s > 12$

As long as $V_s > 12 \Rightarrow$ D is on and $i = \frac{V_s - 12}{100}$

Assume D is oFF.




KVL $\Rightarrow -V_s + 100(0) + V + 12 = 0 \Rightarrow V = V_s - 12 < 0$ to verify oFF.

$\Rightarrow V_s < 12$

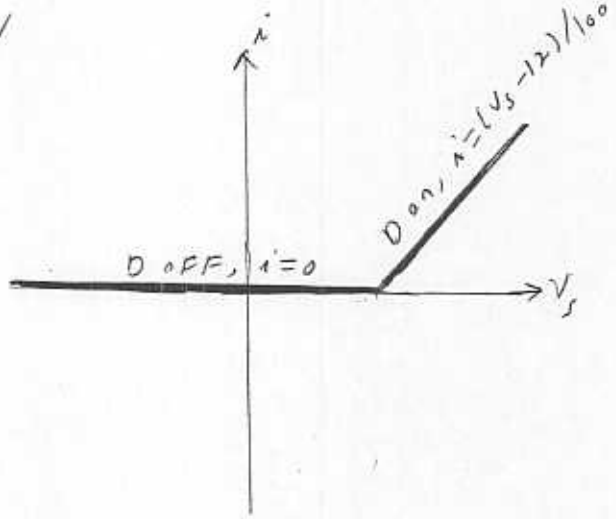
As long as $V_s < 12 \Rightarrow$ D is oFF and $i = 0$.

To plot $i_D \perp V_s$, we know that

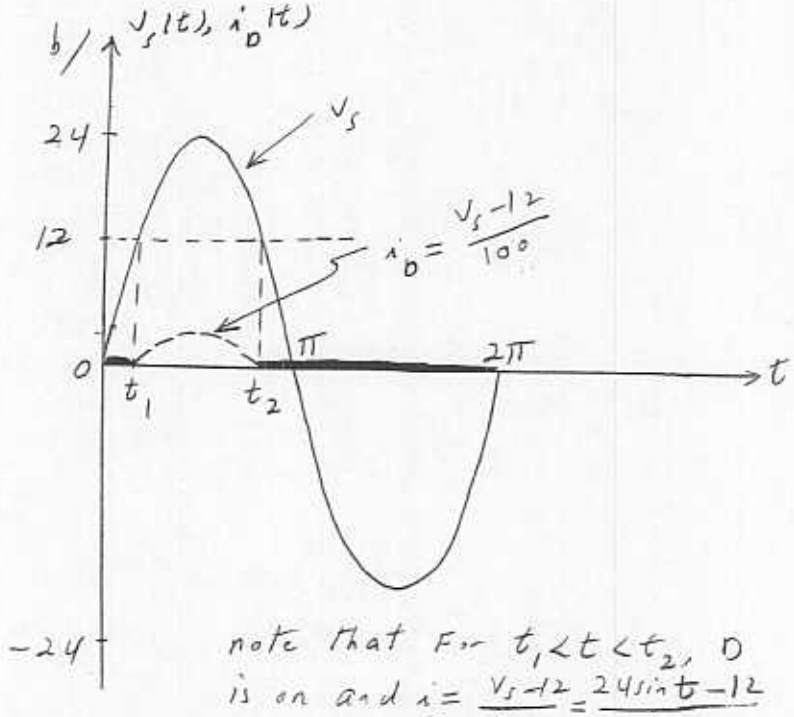
$$\begin{cases} i = \frac{V_s - 12}{100} & \text{when } V_s > 12, \text{ D on} \\ i = 0 & \text{when } V_s < 12, \text{ D oFF} \end{cases}$$

Note that when $V_s = 12$, the diode is operating at the boundary of on and oFF. As soon as $V_s$ changes by a small amount, D goes on or oFF.

a/




b/




note that For $t_1 < t < t_2$, D is on and $i_D = \frac{V_s - 12}{100} = \frac{24\sin t - 12}{100}$

What are the values of $t_1$ and $t_2$?

$24 \sin t = 12 \Rightarrow \sin t = 0.5 \Rightarrow t = \frac{\pi}{6}, \frac{5\pi}{6} \Rightarrow$

$t_1 = \frac{\pi}{6} = \frac{3.14}{6}$ sec, $t_2 = \frac{15.7}{6}$ sec

conduction time $= \frac{15.7}{6} - \frac{3.14}{6}$

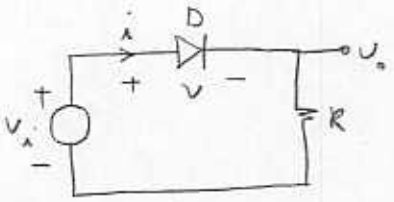
$i_D$(max) happens at $t = \frac{\pi}{2}$ when $V_s = 24$ V.

$$i_D(max) = \frac{V_s(max) - 12}{100} = 0.12 \text{ A}$$

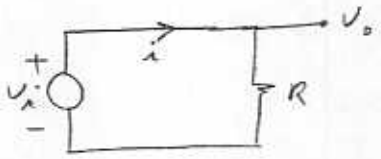
ENGR. 2364
Handout #4

Sections 3.1, 3.2

Ex. plot $V_o$ & $V_i$. plot $V_o(t)$ if $V_i(t) = 12\sin t$.



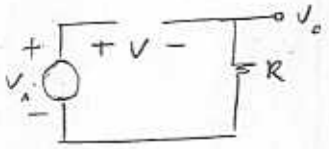

Assume D is on ⇒




$i = \frac{V_i}{R} > 0$ to verify on ⇒ $V_i > 0$

* As long as $V_i > 0$ ⇒ D is on and $V_o = V_i$

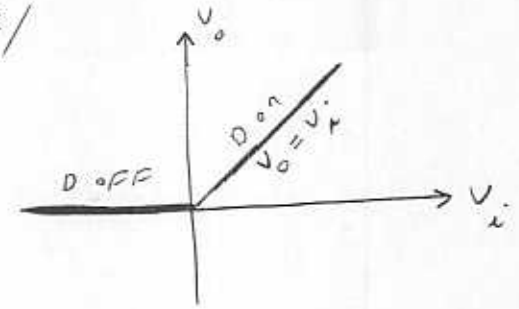
Assume D is OFF.



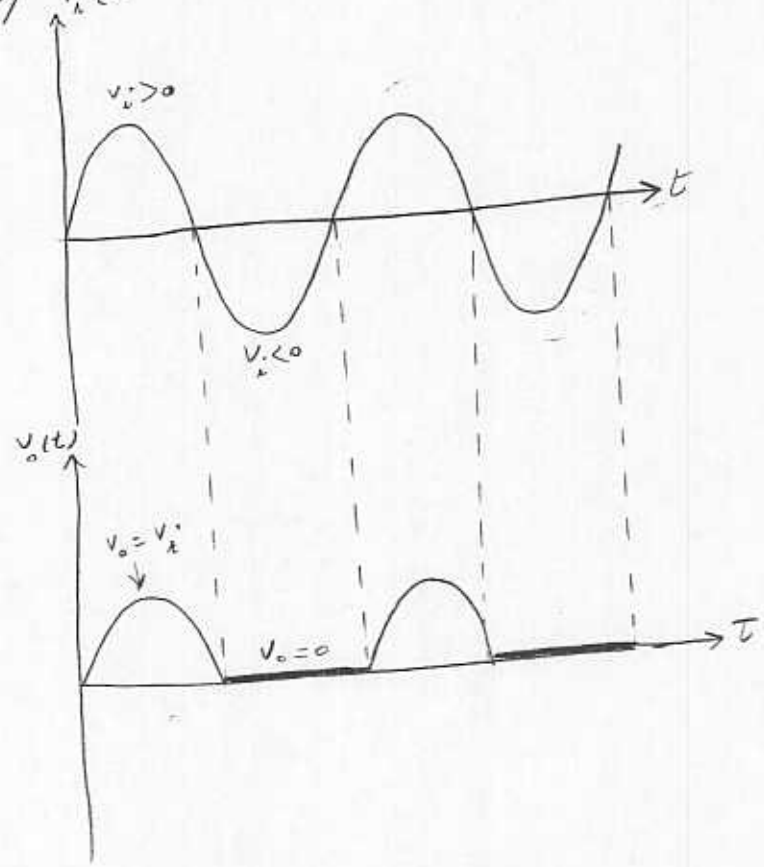

$-V_i + v + R(0) = 0 \Rightarrow v = V_i < 0$ to verify OFF ⇒ $V_i < 0$

* As long as $V_i < 0$ ⇒ D is OFF and $V_o = 0$

a/




b/ $V_i(t)$




This circuit is called a rectifier. When $V_i > 0$, $V_i$ is transfered to the output ($V_o = V_i$). When $V_i < 0$, $V_o = 0$.

## Real diodes:

Real diodes are the diodes that we use in the laboratories to make electronic circuits. They are different from ideal diodes. Ideal diodes make circuit analysis easy but they are not real life diodes.

A real diode has the i-v curve shown below.


$$i = I_s\left(e^{v/nV_T} - 1\right)$$

$I_s$ = saturation current. $I_s$ is of the order of $10^{-15}$ A. $I_s$ is a very strong function of temperature. $I_s$ doubles in value for every 5°C rise in temperature. To show this temperature dependence, we write $I_s(T)$.

$V_T$ = thermal voltage $= \frac{KT}{q}$

$k$ = Boltzmann's constant $= 1.38 \times 10^{-23}$ joules/kelvin

$T$ = the absolute temperature in kelvins = 273 + temperature in °C

$q$ = the magnitude of electronic charge $= 1.602 \times 10^{-19}$ Coulomb

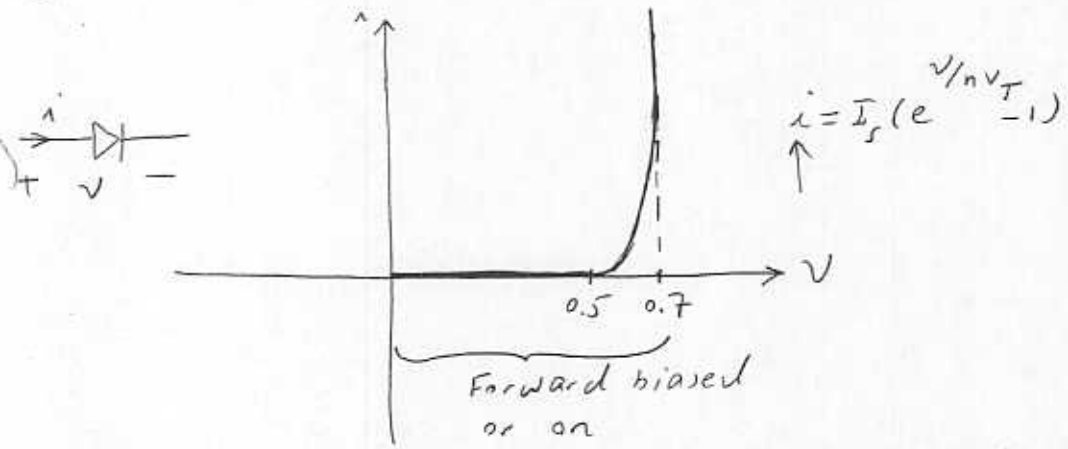
At room temperature (20°C) $\Rightarrow V_T = \frac{1.38 \times 10^{-23}(273+20)}{1.602 \times 10^{-19}} = 25.2\text{mV} \cong 25\text{mV}$

We will use $V_T = 25$mV unless a temperature very different from room temperature is specified.

$n$ = a constant that takes a value between 1 and 2. Diodes in integrated circuits exhibit $n=1$. Discrete diodes have $n=2$.

## Plot of i-v for a real diode:

Forward biased or on region ($v > 0$).




1) Note that current is negligible for $v$ smaller than 0.5 V. This value is called the cut-in voltage.

2) For $0.6 \leq v \leq 0.8$, the diode conducts and can carry a lot of current in the range $v = 0.7$ to $0.8$ V.

EX. A diode has $I_s = 10^{-15}$ A and $v = 0.7$ V.

a/ Find $i$ if $n = 1$.

b/ Find $i$ if $n = 2$.

Solution: For $i \gg I_s$ or $v \gg nV_T$, we neglect the $-1$ term in $i$-$v$ relationship.

$$i \cong I_s e^{v/nV_T} \quad \text{if } i \gg I_s \text{ or } v \gg nV_T$$

a/ $v = 0.7 \gg nV_T = 25\text{mV} \Rightarrow$

$$i = I_s e^{v/nV_T} = 10^{-15} e^{0.7/25\times10^{-3}} = 1.446\text{ mA}$$

note that $i = 1.446\text{mA} \gg I_s = 10^{-12}\text{ mA}$. Therefore, $i \gg I_s$ and $v \gg nV_T$ are consistent with each other.

b/ $v = 0.7 \gg nV_T = 50\text{mV}$

$$i = I_s e^{v/nV_T} = 10^{-15} e^{0.7/50\times10^{-3}} = 1.2\times10^{-9}\text{ A}$$

note $i = 1.2\times10^{-9}\text{ A} \gg 10^{-15}\text{ A}$. $n$ changed by a factor of two and $i$ by a factor of $1.2\times10^{6} \Rightarrow$ value of $n$ is very important in the diode current.

Note that in electronics, we are going to take $a \gg b$ to mean $a$ bigger than $b$ by a factor of at least ten.

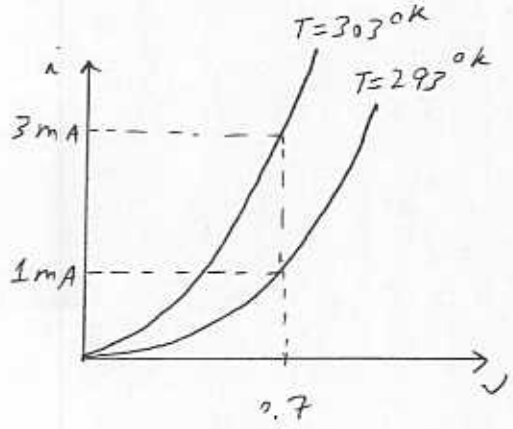
Effect of temperature on $i-v$ curve of a real diode:

$$i = I_s(e^{v/nV_T} - 1)$$

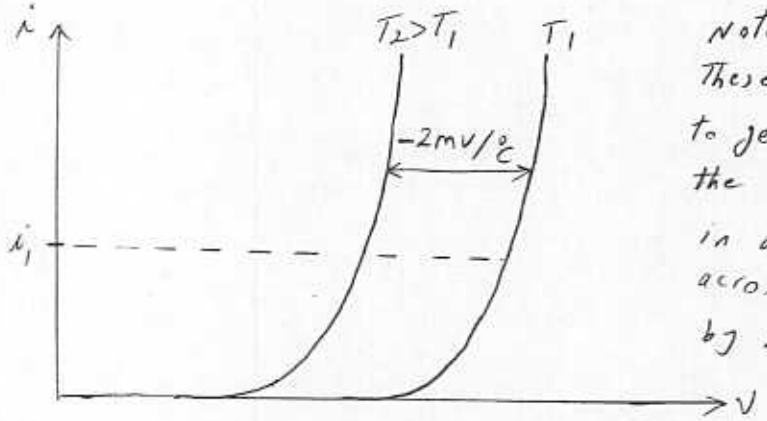
Note that there are two parameters in this equation that vary with temperature: $I_s(T)$ and $V_T = \frac{kT}{q}$.

When the temperature is increased, $i$ will increase in value for a given voltage.

Ex. If at $T = 273 + 20^\circ$, we have $i = 1mA$ for an applied voltage of $0.7V$. Then at $T = 273 + 30^\circ$, we can get $i = 3mA$ for the same applied voltage of $0.7V$.



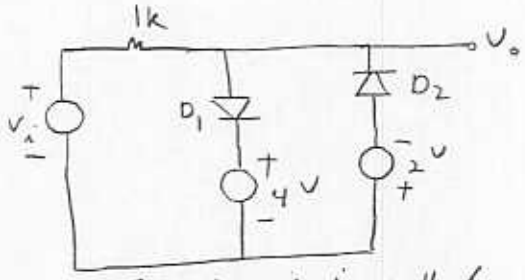

These two curves demonstrate that as $T$ increases, the $i-v$ curve moves to the left to give a higher current for the same voltage. Temperature dependence of a real diode in the forward biased region is shown below.




Note that another way to look at these $i-v$ curves is to say that to generate a current $i_1$ through the diode, for every $1^\circ C$ increase in diode temperature, the voltage across the diode can be decreased by $2mV$. In other words, since we have increase temperature by $1^\circ C$, we can decrease the voltage across the diode by $2mV$ and still [illegible]

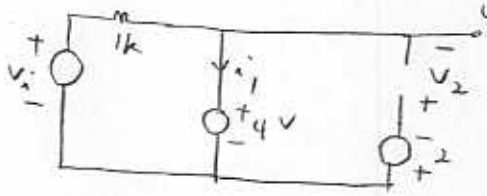
Handout #5

Ex. Find and plot $v_o$ vs $v_i$.
plot $v_o(t)$ if $v_i(t) = 12\sin\omega t$.




This circuit is called a limiter.

1) Assume $D_1$ on, $D_2$ OFF.



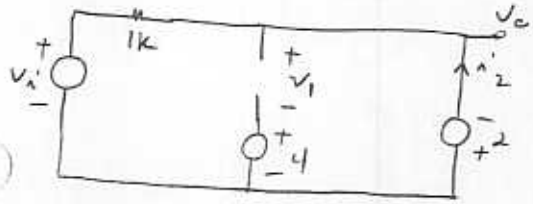

KVL $\Rightarrow -v_i + 1k\,i_1 + 4 = 0 \Rightarrow$

$$i_1 = \frac{v_i - 4}{1k} > 0 \Rightarrow v_i > 4$$

KVL $\Rightarrow -4 - v_2 - 2 = 0 \Rightarrow v_2 = -6 < 0$ ✓

* As long as $v_i > 4 \Rightarrow D_1$ on, $D_2$ OFF & $v_o = 4$ V

2) Assume $D_1$ OFF, $D_2$ on

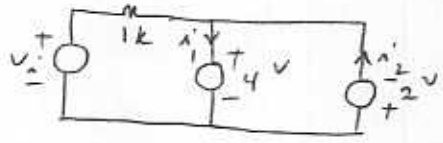



KVL $\Rightarrow +2 + 1k\,i_2 + v_i = 0 \Rightarrow i_2 = \frac{-v_i - 2}{1k} > 0 \Rightarrow v_i < -2$

KVL $\Rightarrow +2 + v_1 + 4 = 0 \Rightarrow v_1 = -6 < 0$ ✓

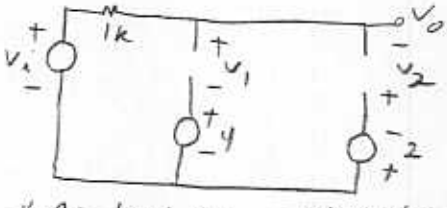
* As long as $v_i < -2 \Rightarrow D_1$ OFF, $D_2$ on & $v_o = -2$ V

3) Assume both diodes on




This can not happen because KVL does not hold.
KVL $\Rightarrow -4 - 2 = 0$ ? X
In this circuit, both diodes will not be on at the same time.

4) Assume both diodes off

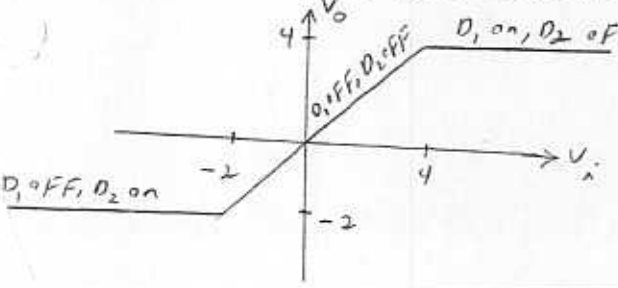


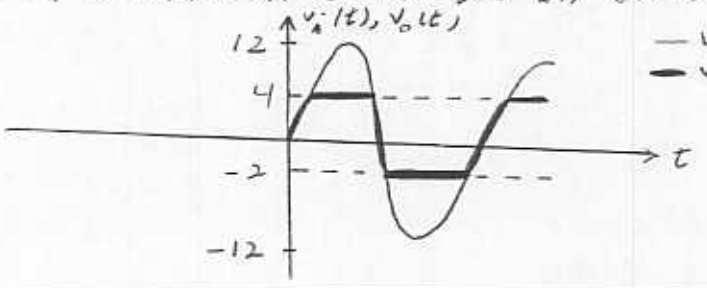

KVL $\Rightarrow -v_i + 1k(0) + v_1 + 4 = 0 \Rightarrow v_1 = v_i - 4 < 0 \Rightarrow v_i < 4$

KVL $\Rightarrow -v_i + 1k(0) - v_2 - 2 = 0 \Rightarrow v_2 = -v_i - 2 < 0 \Rightarrow v_i > -2$

* As long as $-2 < v_i < 4 \Rightarrow D_1$ OFF, $D_2$ OFF and $v_o = v_i$

Note that different limits obtained for $v_i$ in different cases are all consistent.



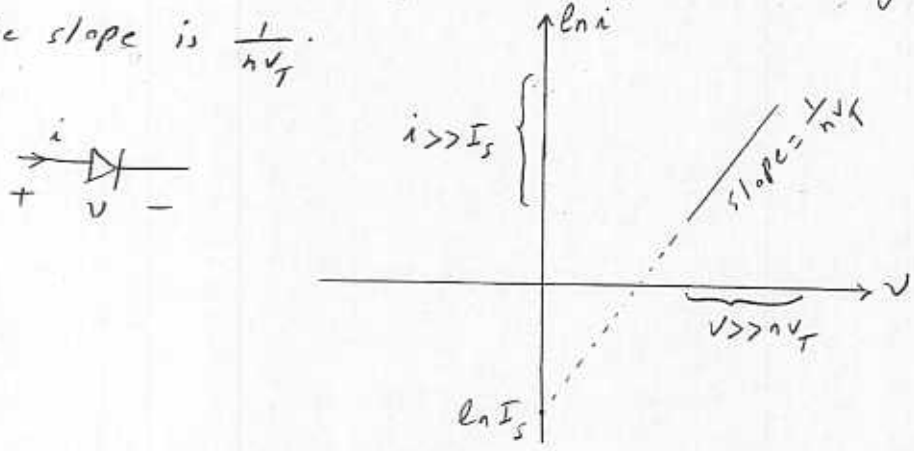



# ENGR. 364
## Handout #6

Remember that if $v >> nV_T$ or $i >> I_S$, we can write

$$i \cong I_S e^{v/nV_T} \Rightarrow v \cong nV_T \ln\frac{i}{I_S} \Rightarrow \ln i \cong \ln I_S + \frac{v}{nV_T}$$

This implies that for $i >> I_S$ or $v >> nV_T$, $\ln i$ changes linearly with $v$ and the slope is $\frac{1}{nV_T}$.




At a voltage of $v_1$, let the current through the diode be $i_1$. i.e., $i_1 = I_S e^{v_1/nV_T}$

at a voltage of $v_2$, let the current through the diode be $i_2$. i.e., $i_2 = I_S e^{v_2/nV_T}$

Note that we are assuming $i_1 \& i_2 >> I_S$ or $v_1 \& v_2 >> nV_T$ To use the approximate equation. we know have

$$\frac{i_2}{i_1} = e^{(v_2 - v_1)/nV_T} \Rightarrow \underline{\underline{v_2 - v_1 = nV_T \ln\frac{i_2}{i_1}}}$$

or in terms of base-10 logarithms,

$$\log_{10}\frac{i_2}{i_1} = \log_{10} e^{(v_2-v_1)/nV_T} = (v_2 - v_1)/nV_T \log_{10} e \Rightarrow$$

$$\underline{\underline{v_2 - v_1 = 2.3nV_T \log_{10}\frac{i_2}{i_1}}}$$

Ex. Assume that for a given diode $n = 1$. If the current through the diode is to increase from a value of $i_1$ to $10i_1$, how much do we need to increase the voltage across the diode. Assume $i_1 >> I_S$

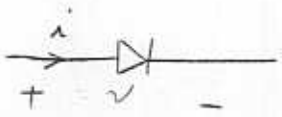
Solution: Initially, we have a voltage of $v_1$ and a current of $i_1$. Suppose $i_2 = 10i_1$ corresponds to the voltage $v_2$. we have

$$v_2 - v_1 = 2.3(1)(25m)\log_{10} 10 = 57.5mv = 0.0575^{v}$$

Notice how sensitive a diode is to a change of voltage across it. It only takes a voltage of about 0.06 V to change the current flow through the diode by a factor of 10. Diodes have the most sensitive $i$-$v$ curve.

Reverse-bias region:

The reverse-bias region for a real diode is also the region identified by $v<0$ like an ideal diode. The $i$-$v$ equation described above for the real diode in the forward-bias region holds in the reverse bias region.

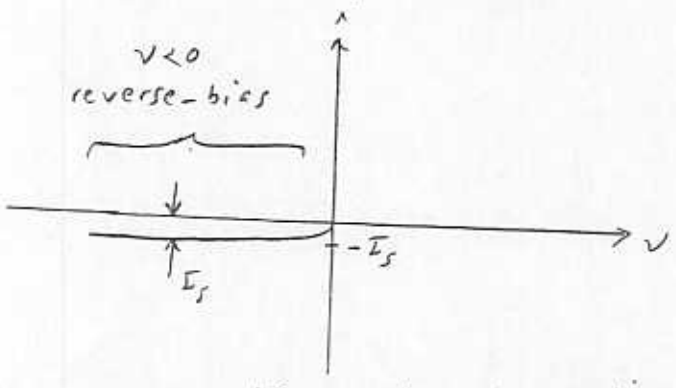



$$i = I_s\left(e^{v/nV_T} - 1\right)$$

Note that $v<0$ in the reverse-bias region. If $|v|$ is bigger than $nV_T$ by a few times, then we have

$$e^{v/nV_T} \cong 0 \Rightarrow \quad i = -I_s$$

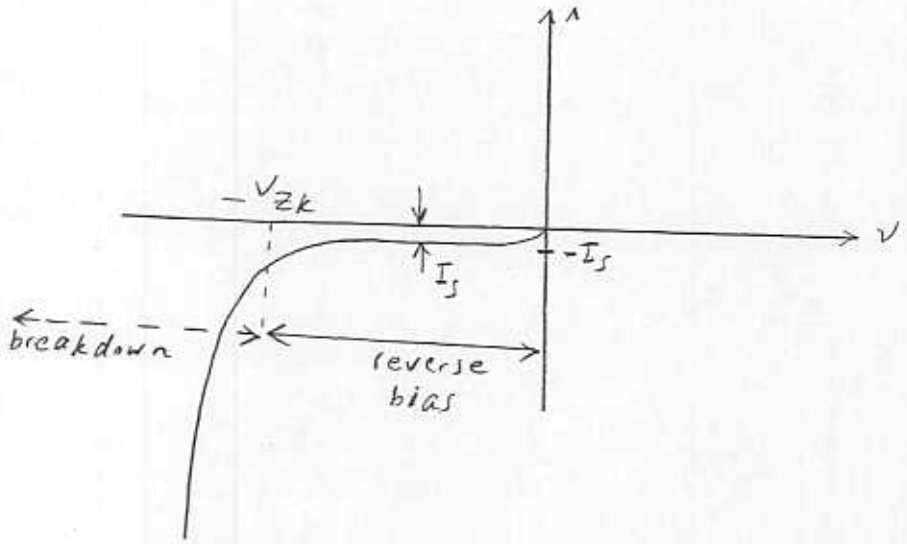
We usually take $i = -I_s$ to be the current for a real diode in the reverse-bias region even if $|v|$ is not a few times bigger than $nV_T$.




Note that in the reverse-bias region, conventional $i$ and $v$ are both negative.

Breakdown region:

When the magnitude of the reverse-bias voltage ($v<0$) exceeds a threshold value, the reverse current $i<0$ becomes much larger than $-I_S$.



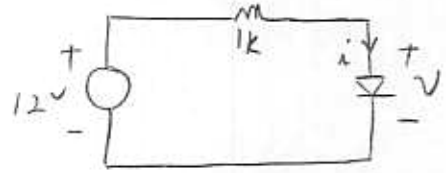

This threshold value is called the breakdown voltage and is denoted by $V_{Zk}$. The diode is said to enter Zener breakdown and K stands for knee. Note that in the breakdown region, we have $v<0$ and $i<0$.

Also note that the breakdown voltage $V_{Zk}$ is defined as a positive voltage.

Note that in the breakdown region, the diode does not follow the $i-v$ curve $i = I_S(e^{v/nV_T} - 1)$ which holds in the forward and reverse biased regions.

Analysis of circuits containing real diodes:

Ex.




$n = 1$

$I_S = 10^{-15}$ A

A) numerical solution:

$$i = I_s\left(e^{V/nV_T} - 1\right) \Rightarrow i = 10^{-15}\left(e^{V/25m} - 1\right) = 10^{-15}\left(e^{40V} - 1\right)$$

if we assume $i \gg I_s$ or $V \gg nV_T$, we have

$$i \cong 10^{-15} e^{40V}$$

$$KVL \Rightarrow -12 + 1k\,i + V = 0$$

$$\begin{cases} i = 10^{-15} e^{40V} \\ i = \dfrac{12 - V}{1k} \end{cases} \Rightarrow 10^{-15} e^{40V} = \frac{12 - V}{1k} \quad (1)$$

Now, you can use a numerical technique to find V or just choose different values of V until the value that satisfies eq. 1 is found (trial and error).

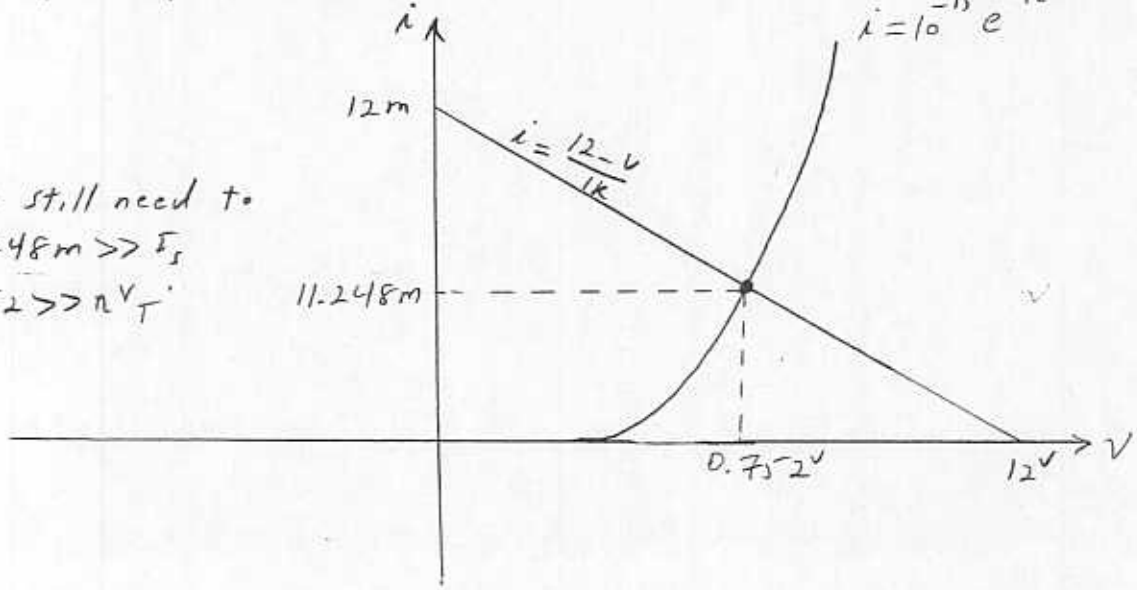
After many trials, I found $V \cong 0.752^V \Rightarrow i = \frac{12 - V}{1k} = 11.248mA$

Now, check the assumption we made at the beginning. i.e, $i \gg I_s$ or $V \gg nV_T$.

$i = 11.248mA \gg I_s$ or $V = 0.752 \gg nV_T = 25mV$

B) Graphical solution:

The voltage and current of the diode have to satisfy two curves. one is $i = I_s\left(e^{V/nV_T} - 1\right) = 10^{-15}\left(e^{40V} - 1\right) \cong 10^{-15} e^{40V}$ and the other one is the KVL equation $i = \frac{12 - V}{1k}$. Therefore, the operating point of the diode (i.e, i and V values) is the point of intersection of the two curves.




Note that we still need to verify $i = 11.248m \gg I_s$ or $V = 0.752 \gg nV_T$.

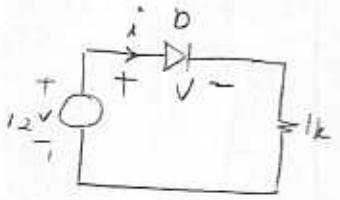
ENGR. 364
Handout #7

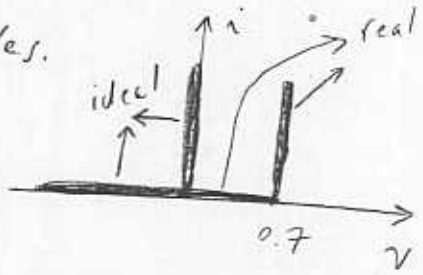
Comparison of ideal and real diodes:

A) Forward-bias region:

For an ideal diode, this region corresponds to where $v=0$ and $i>0$.
For a real diode, this region corresponds to where $v>0$ and $i>0$.
Since a real diode can carry all currents of interest at about 0.7 V, we take $v=0.7^{V}$ to be the typical voltage in the following discussion.

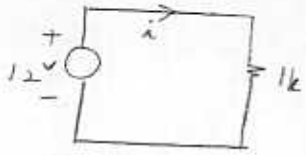
Ex. Find $v$ and $i$ assuming ideal and real diodes.




a/ ideal diode:

Assume on ⇒

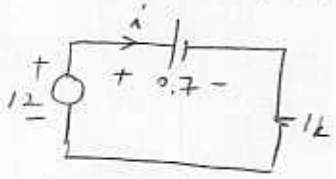



$i=\frac{12}{1k}=12mA>0$ ✓

Therefore, $v=0, i=12m$

b/ real diode

Assume on with $v_{typical}=0.7^{V}$

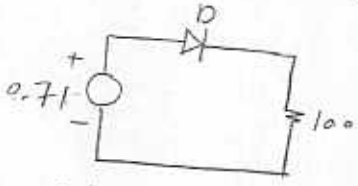



$-12+0.7+1k\,i=0 \Rightarrow$

$i=11.3mA>0$ ✓

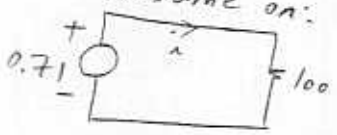
Therefore, $v=0.7, i=11.3^{mA}$

Ex. Repeat the previous problem for the circuit shown below.




a/ ideal diode:

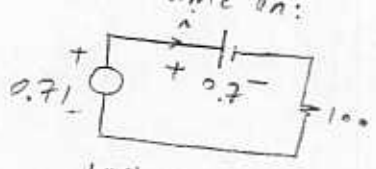
Assume on:




$i=\frac{0.71}{100}=7.1mA>0$ ✓

b/ real diode:

Assume on:



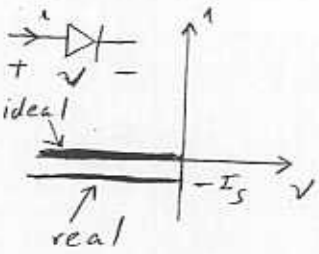

KVL $\Rightarrow -0.71+0.7+100\,i=0 \Rightarrow$

$i=1mA>0$ ✓

Currents are now very different. When the input ...

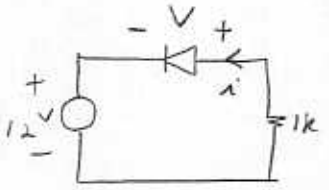
to 0.7 V, whether we assume real or ideal diode makes a significant difference in current.

B) Reverse-bias region:



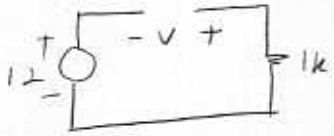

$i = 0$ ideal
$i = -I_S$ real

Ex. Find $v$ and $i$ assuming ideal and real diodes:




a/ ideal diode:

Assume OFF:



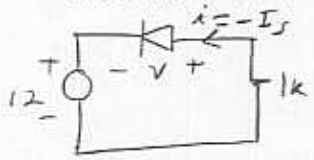

KVL $\Rightarrow -12 - v = 0 \Rightarrow$

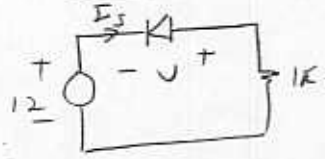
$v = -12 < 0$ ✓

$\Rightarrow v = -12, i = 0$

b/ real diode: (take $I_S = 10^{-15}$ A).

Assume OFF:




KVL $\Rightarrow -12 - v + 1000(10^{-15}) = 0 \Rightarrow$

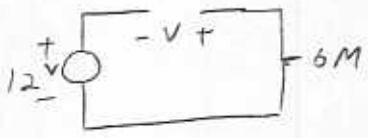
$v \cong -12 < 0$ ✓

$\Rightarrow v = -12, i \cong -10^{-15}$ A

Ex. Repeat the previous example if $I_S = 1$ μA and 1k is replaced by a 6M resistor.

a/ ideal diode:

Assume OFF:



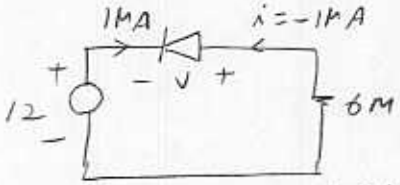

KVL $\Rightarrow -12 - v + 6M(0) = 0 \Rightarrow$

$v = -12 < 0$ ✓

$\Rightarrow v = -12, i = 0$

b/ real diode:

Assume OFF




KVL $\Rightarrow -12 - v + 6M(1M) = 0 \Rightarrow$

$v = -6 < 0$ ✓

$\Rightarrow v = -6, i = 1$ μA

The voltages are significantly different. When the product of resistor values in the circuit and saturation current of diode is significant (of the order of a few tenth of a volt or higher), it makes a

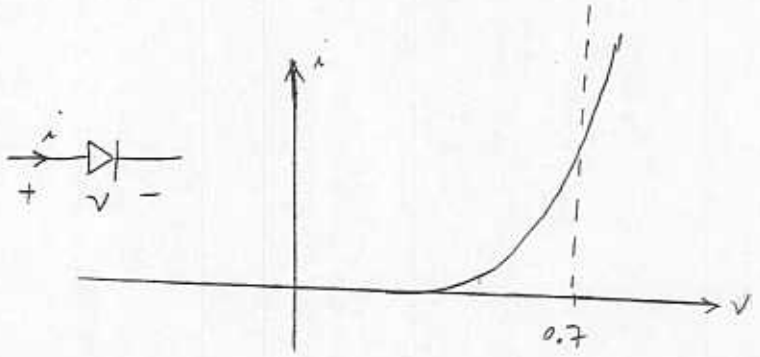
difference whether we assume ideal or real diodes.

Models of diodes based on real diode equation $i = I_s(e^{v/nV_T} - 1)$.

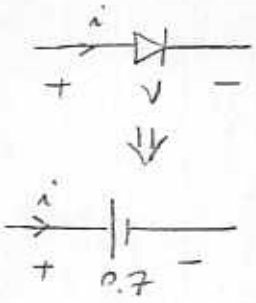
The idea here is to find circuit models of diodes that better approximate a real diode ($i = I_s(e^{v/nV_T} - 1)$) than an ideal diode. We try to avoid using the $i$-$v$ equation of a real diode because it is too complicated. We try to find models that closely approximate it and are easier to work with in a circuit.

A) Constant battery model:

In this case, the $i$-$v$ curve of the real diode is approximated by the dashed line.

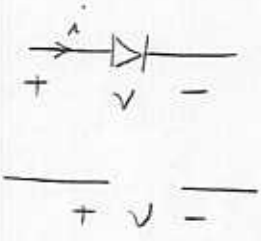



Forward-bias region



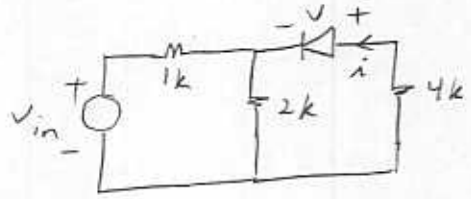

verify $i > 0$

reverse-bias region (ignore $I_s$)

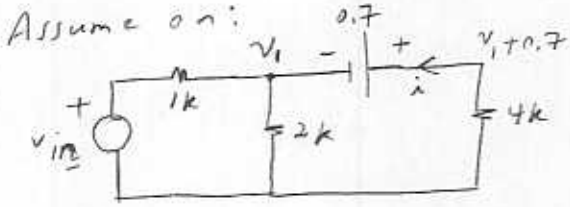



verify $v < 0.7$

Ex. Find and plot $i$ & $v_{in}$ for the circuit shown below. Assume a constant battery model with $V = 0.7^V$.




Assume on:



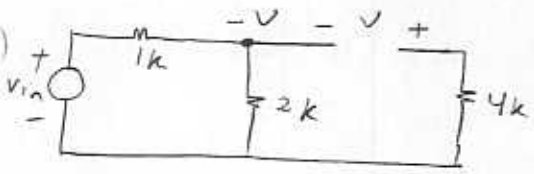

KCL $\Rightarrow \frac{v_1 - v_{in}}{1k} + \frac{v_1}{2k} + \frac{v_1 + 0.7}{4k} = 0 \Rightarrow v_1 = \frac{4v_{in} - 0.7}{7}$

$i = -\frac{v_1 + 0.7}{4k} = -\frac{4v_{in} + 4.2}{28k} > 0 \Rightarrow$

$4v_{in} + 4.2 < 0 \Rightarrow v_{in} < -1.05^V$

As long as $v_{in} < -1.05 \Rightarrow$ D is on and $i = -\frac{4v_{in} + 4.2}{28k}$

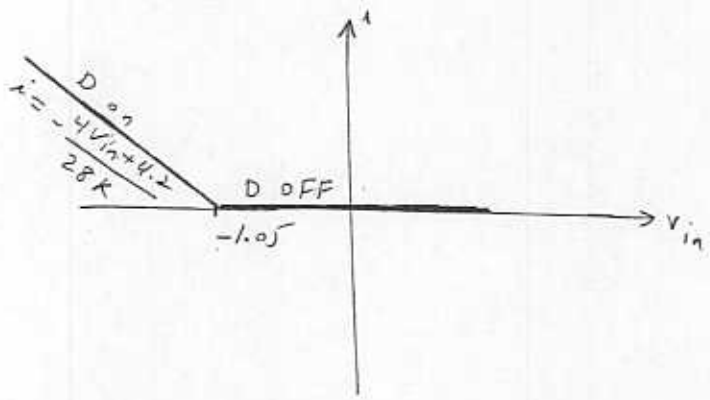
Assume OFF:




$$KCL \Rightarrow \frac{-V-v_{in}}{1k} + \frac{-V}{2k} = 0 \Rightarrow \quad V = -\frac{2}{3} v_{in} < 0.7 \Rightarrow$$

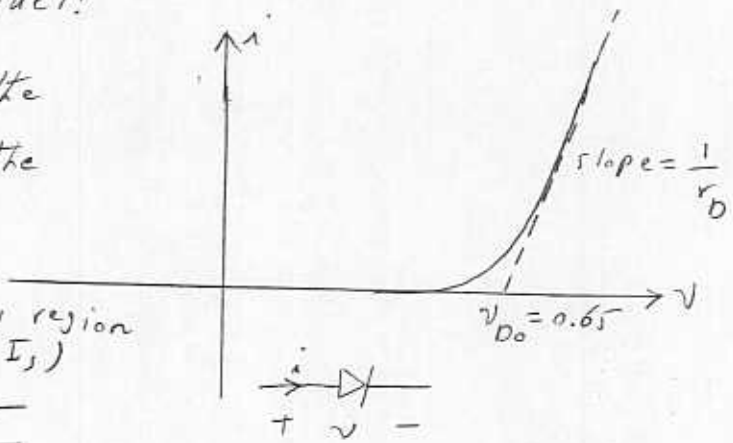
$$v_{in} > -1.05\text{V}$$

As long as $v_{in} > -1.05 \Rightarrow$ D is OFF and $i = 0$

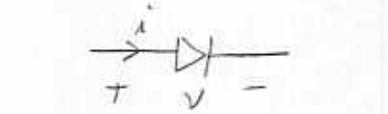


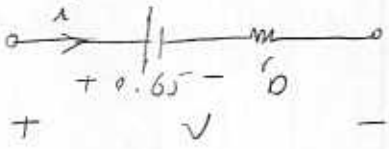

B) Constant battery and resistor model:

In this case, the i-v curve of the real diode is approximated by the dashed line.



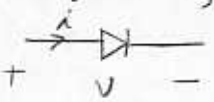

Forward-bias region




verify $i > 0$

reverse-bias region (neglect $I_s$)

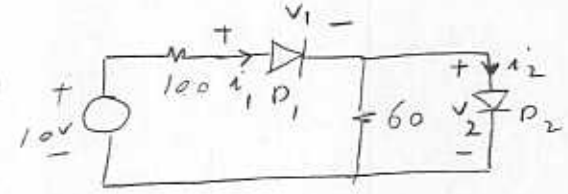




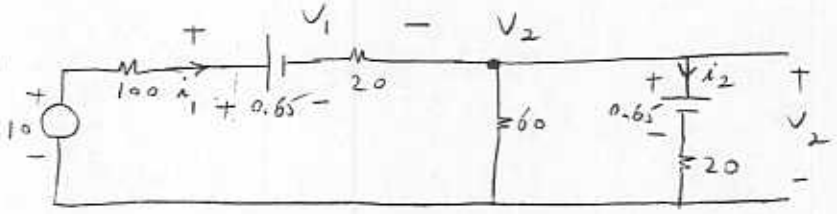
verify $v < 0.65$




Ex. Use the piecewise-linear model (constant battery and resistor model) and Find $v_1, v_2, i_1$ and $i_2$. ($V_D = 0.65$, $r_D = 20\Omega$)



Assume both diodes on:




KCL $\Rightarrow \frac{V_2 - 10 + 0.65}{120} + \frac{V_2}{60} + \frac{V_2 - 0.65}{20} = 0 \Rightarrow V_2 = 1.27^{V}$

$i_1 = \frac{9.35 - 1.27}{120} = 67.3mA > 0$ ✓

$i_2 = \frac{V_2 - 0.65}{20} = 31mA > 0$ ✓

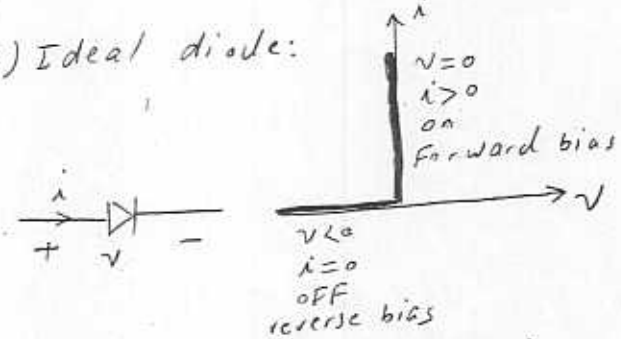
$V_1 = 0.65 + 20 i_1 = 1.99^{V}$ = voltage across $D_1$

$V_2 = 1.27^{V}$ = voltage across $D_2$

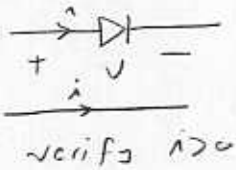
# ENGR.364
## Handout #8

Diode models in a nutshell:

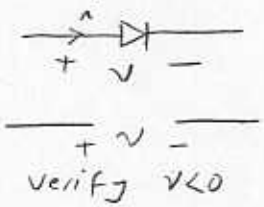
A) Ideal diode:



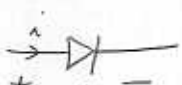

IF you assume on



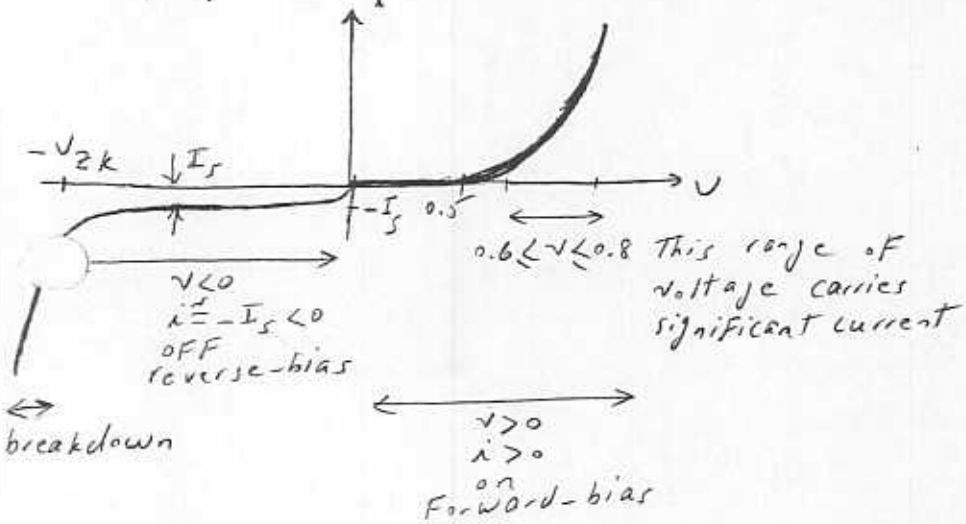

IF you assume oFF




B) Real diode (most realistic model):



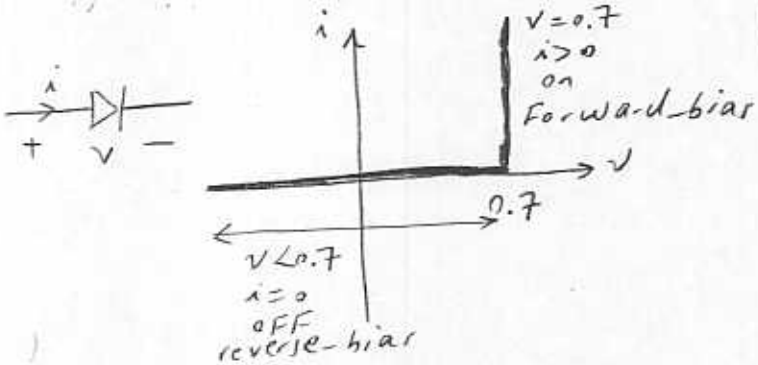

$i = I_s(e^{v/nV_T} - 1)$



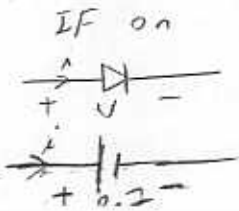

Note: A real diode modeled by $i = I_s(e^{v/nV_T} - 1)$ is hard to work with. It results in equations that has to be solved by trial and error. We can find models for a real diode based on $i = I_s(e^{v/nV_T} - 1)$ which are easier to work with and are also more realistic than an ideal diode model.

C) diode models based on the i–v relationship of a real diode:

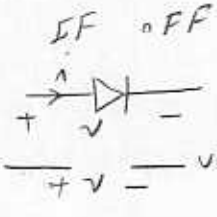
1) Constant battery model:



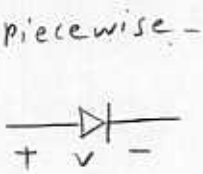

IF on

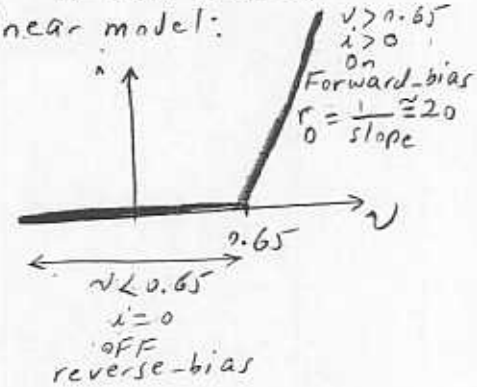



IF oFF

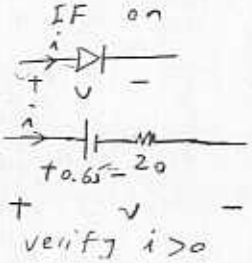



2) Piecewise-linear model:

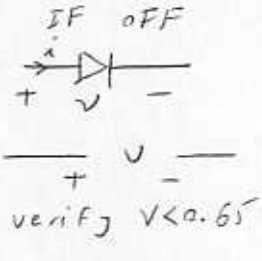



IF on

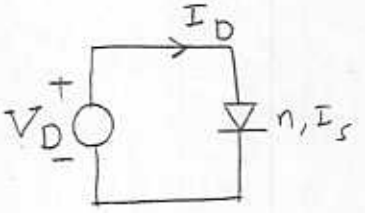



IF oFF

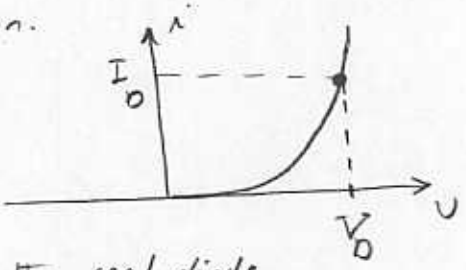


Small signal model of a real diode:

There are applications in which a diode is biased to operate at a DC operating point in the forward-bias region.

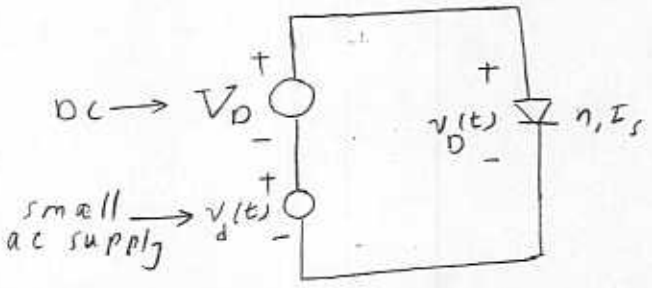



$$I_D = I_S\left(e^{V_D/nV_T} - 1\right)$$




The DC power supply $V_D$ generates $I_D$ through the real diode

Next, we superimpose a small ac supply on the DC power supply.

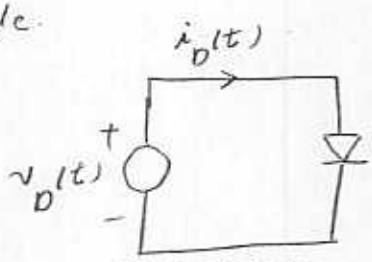



We want to find how the diode responds to $v_d(t)$. In other words, what is the current that flows through the diode due to $v_d(t)$.

total voltage across diode $= v_D(t) = V_D + v_d(t)$

↑ DC + AC ; ↑ DC ; ↑ AC

This total voltage $v_D(t)$ generates a current of $i_D(t)$ through the diode.




without application of $v_d(t)$ $\Rightarrow I_D = I_S e^{V_D/nV_T}$ assuming $V_D \gg nV_T$

with $v_d(t)$ applied $\Rightarrow v_D(t) = V_D + v_d(t)$ = total voltage

$i_D(t) = I_S e^{v_D(t)/nV_T}$ assuming $v_D(t) \gg nV_T$

$$i_D(t) = I_S e^{(V_D + v_d)/nV_T} = I_S e^{V_D/nV_T} e^{v_d/nV_T} = I_D e^{v_d/nV_T}$$

Note that we can write $e^x \cong 1 + x$ if $x \ll 1$ ($x_{max} \cong 0.1$) Remember lol

$e^{v_d/nV_T} \cong 1 + \frac{v_d}{nV_T}$ if $\frac{v_d}{nV_T} \ll 1 \Rightarrow \left.\frac{v_d}{nV_T}\right|_{max} = 0.1 \Rightarrow \left.v_d\right|_{max} = 0.1nV_T$

Since our definition of much smaller or much bigger is a factor of ten, $\frac{v_d}{nV_T}$ can be at most 0.1. This means that the AC supply can be at most $\left.v_d(t)\right|_{max} = 0.1nV_T$ For $e^{v_d/nV_T} \cong 1 + \frac{v_d}{nV_T}$ to be valid. At no time t

the ac supply can become larger than $0.1nV_T$. This is what we mean by a small signal AC voltage across the diode.

$$i_D(t) = I_D e^{v_d/nV_T} \cong I_D\left(1 + \frac{v_d}{nV_T}\right) = I_D + \frac{I_D}{nV_T} v_d \quad \text{if } v_d \ll nV_T \left(v_d\big|_{max} \cong 0.1nV_T\right)$$

Now, let's investigate our result.

$v_D(t)$ = total applied voltage $= V_D + v_d(t)$

DC AC

$i_D(t)$ = total resulting current $= I_D + \frac{I_D}{nV_T} v_d$

DC AC

We know that the DC voltage $V_D$ results in the DC current $I_D$. From the expressions for $v_D(t)$ and $i_D(t)$ above, it is clear that the AC input $v_d(t)$ results in the AC current $i_d(t) = \frac{I_D}{nV_T} v_d(t)$.

What we have done here is to first apply a DC voltage $V_D$ across the diode to generate the DC current $I_D$. Next, on this DC voltage $V_D$, we superimpose a small signal AC voltage $v_d(t)$ $\left[v_d(t) \ll nV_T\right]$. One to application of $v_d(t)$ on top of $V_D$, the diode generates a current of $i_d(t) = \frac{I_D}{nV_T} v_d(t)$.

Note that the relationship between $i_d$ and $v_d$ is linear exactly the same as that of a resistor. $\left(i_d = \frac{I_D}{nV_T} v_d = \frac{1}{r_d} v_d\right)$

$r_d$ = diode small signal resistance $= \frac{v_d}{i_d} = \frac{nV_T}{I_D}$.

For small AC supplies superimposed on a DC operating point of $V_D$ and $I_D$, the diode acts like a resistor of value $\frac{nV_T}{I_D}$. We can look at this whole process as a superposition problem. There are two power supplies applied to the diode. With the DC supply present only,

The diode generates a current of $I_D$. With the AC supply acting alone, the diode acts like a resistor of value $r_d = \frac{nV_T}{I_D}$ giving a current of $i_d = \frac{I_D}{nV_T} v_d$. The total current is then the sum of the two currents.

$$i_D = I_D + i_d = I_D + \frac{I_D}{nV_T} v_d$$

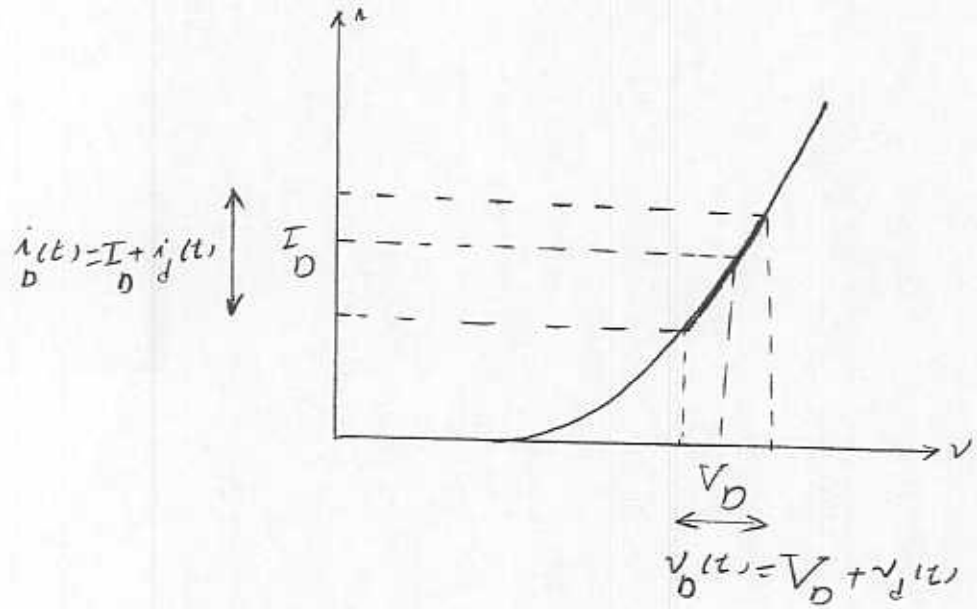
Note that the value of the resistor seen by the AC supply depends on $I_D$ which is established through the diode by the DC voltage $V_D$.

Note: Do not confuse $r_D$ with $r_d$. $r_D$ is the resistor used in piece-wise linear model approximation to a real diode.

$r_d$ is the small signal model of a diode. They are different things!

Small signal model of a diode continued:

Once a DC operating point is established ($V_D, I_D$) using a DC power supply, the diode acts like a resistor of value $r_d = \frac{nV_T}{I_D}$ for all small AC voltages $v_d(t) << nV_T$ that appear across it. The diode then generates a current of $i_d(t) = \frac{v_d(t)}{r_d}$. This is to say that for small variations in diode voltage about a DC value of $V_D$, the diode acts like a resistor.

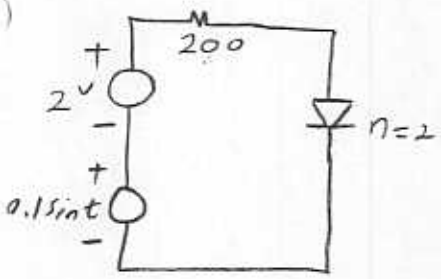



The value of $r_d$ can also be found from the slope of the i-v curve at the point ($V_D, I_D$) because this slope shows how small variations in v around $V_D$ would change i around $I_D$.

$$i = I_s\left(e^{v/nV_T} - 1\right) \cong I_s e^{v/nV_T} \Rightarrow$$

$$\frac{\partial i}{\partial v} = \frac{I_s}{nV_T} e^{v/nV_T} = \frac{i}{nV_T} \Rightarrow r_d^{-1} = \left.\frac{\partial i}{\partial v}\right|_{\substack{v = V_D \\ i = I_D}} = \frac{I_D}{nV_T}$$ same as before.

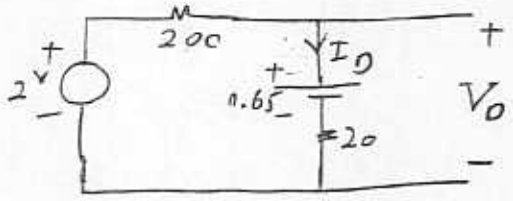
Ex. For the circuit shown below, Find $i_d(t)$ and $v_d(t)$.




we assume the diode can be characterized by a piecewise linear model with $V_{D_0} = 0.65$, $r_D = 20\Omega$.

*Note that $i_d(t)$ and $v_d(t)$ are the AC component of diode's voltage and current.

Solution: First, just consider the DC supply.




Assume D. is on $\Rightarrow$

$-2 + 200 I_D + 0.65 + 20 I_D = 0 \Rightarrow I_D = 6.13mA > 0$ ✓

$V_D = 0.65 + 20 I_D = 0.7726\ V$

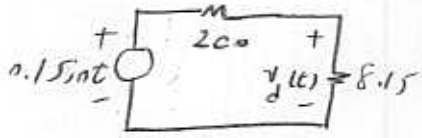
we have found the DC operating point assuming piecewise linear model.

For the AC supply, we assume small signal approximation holds.

$r_d = \frac{nV_T}{I_D} = \frac{2(25m)}{6.13m} = 8.15 \neq r_D$ Note that $r_D$ and $r_d$ are different. $r_D$ is a part of the piecewise linear model describing the behavior of the diode For large DC or AC power supplies. Note that $r_d = \frac{nV_T}{I_D}$ assumes $I_D \gg I_S$ or $V_D \gg nV_T$. We need to verify this.

$V_D = 0.7726 \gg nV_T = 50mV$

For the AC supply, we have




$v_d(t) = \frac{8.15}{208.15} 0.1 \sin t = 3.9 \sin t\ mV$

$v_d(t)\big|_{max} = 3.9mV \ll nV_T = 50mV$

small signal approximation is valid.

In other words, we are allowed to model the diode by $r_d$ because $v_d(t) \leq 0.1 nV_T = 5mV$.

$i_d(t) = \frac{0.1 \sin t}{208.15} = 0.48 \sin t\ mA$

$v_D(t) = 0.7726 + 0.0039 \sin t \ V$

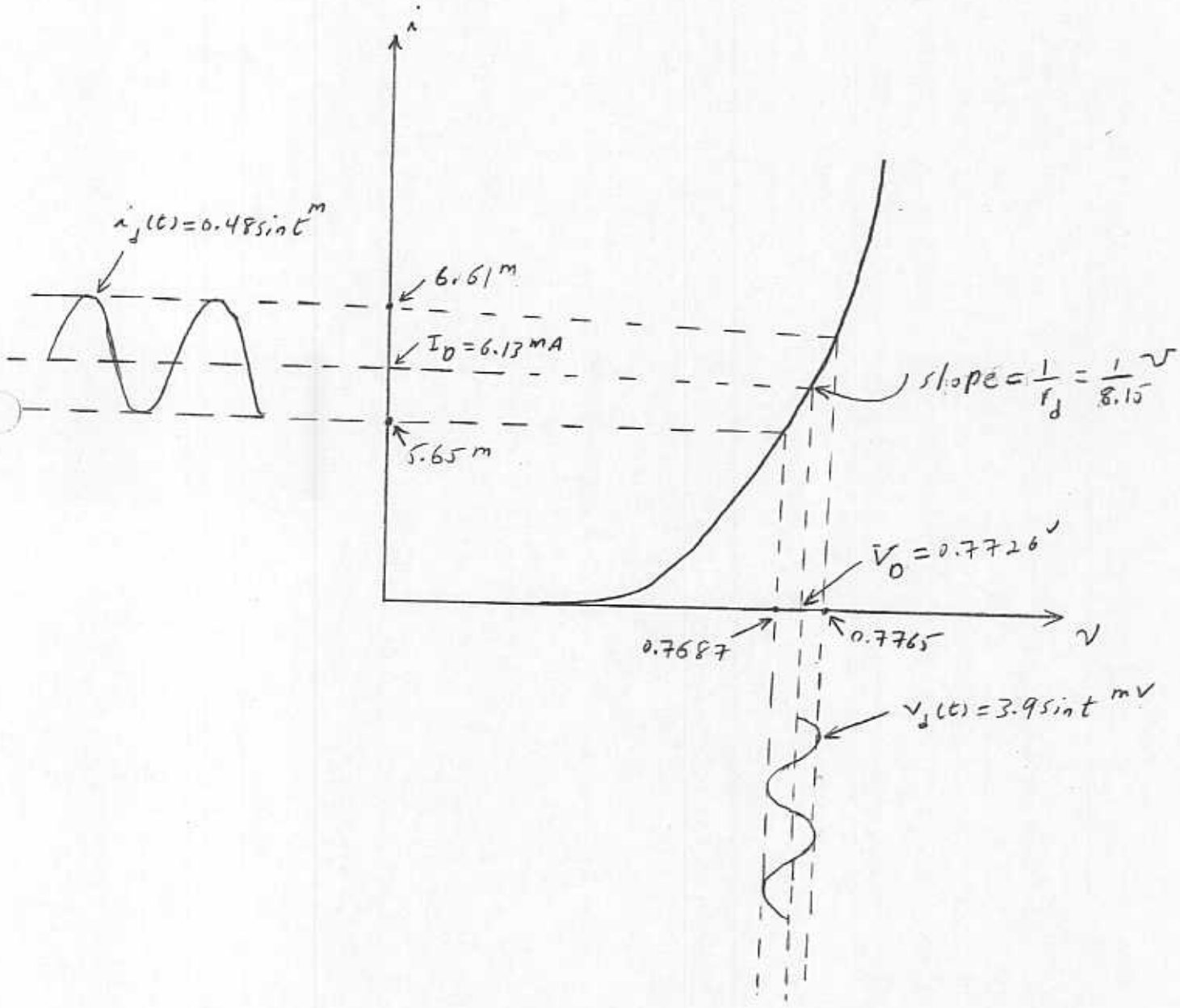
$i_D(t) = 6.13 + 0.48 \sin t \ mA$

$V_0 = 0.7726 \ V$

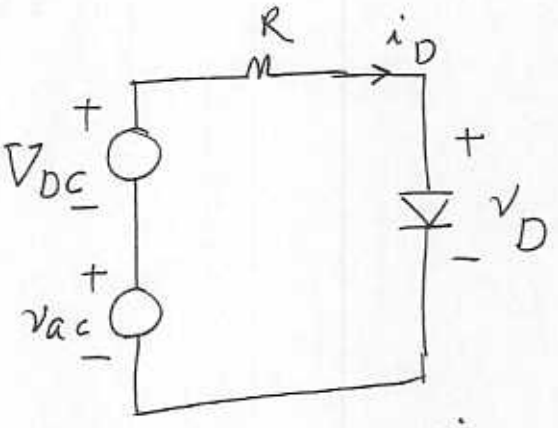
$I_0 = 6.13 \ mA$

$v_d(t) = 3.9 \sin t \ mV$

$i_d(t) = 0.48 \sin t \ mA$



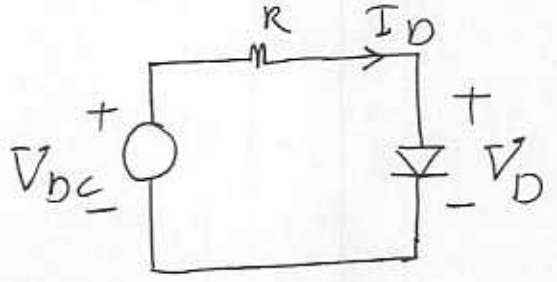
small signal model of a diode in a nutshell:



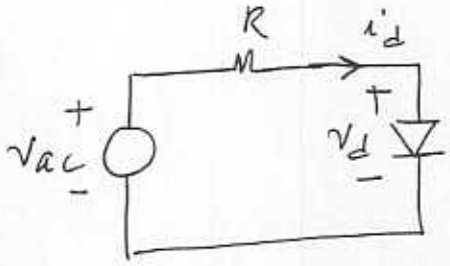

$$v_D = V_D + v_d$$

$$i_D = I_D + i_d$$

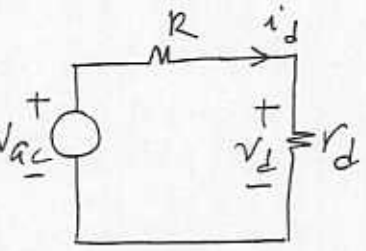
Use superposition To Find $v_D$ and $i_D$.




For the diode, we can use ideal, const. battery, piece-wise linear or the actual ($I_D = I_S[e^{V_D/nV_T} - 1]$) equation.




$$r_d = \frac{nV_T}{I_D} \Rightarrow$$



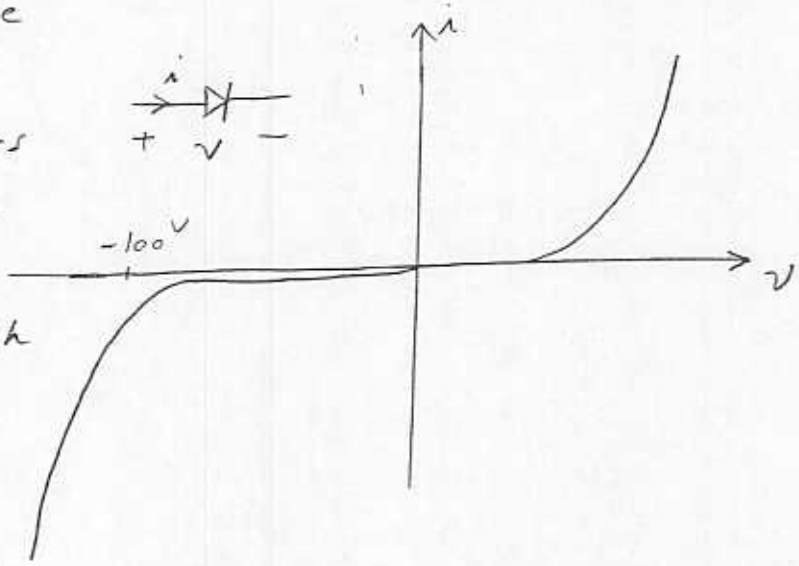

Then $v_D = V_D + v_d$, $i_D = I_D + i_d$

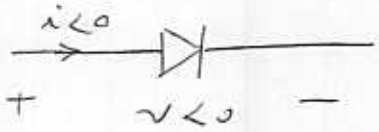
verify $V_D \gg nV_T$, $v_d\big|_{max} \leq 0.1\, nV_T$

55A

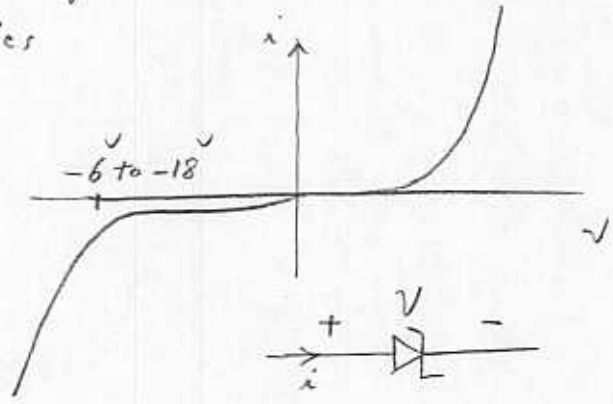
Diodes operating in breakdown:

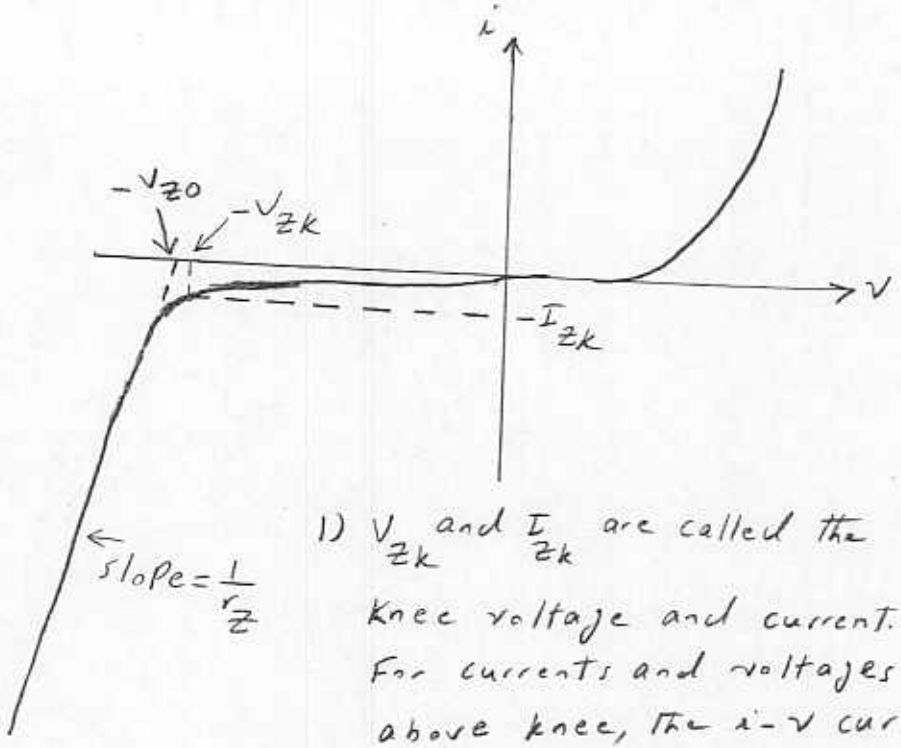
For a real diode, we have the following $i$-$v$ curve. At values of $v$ negative and large in magnitude ($v < -100$), the diode enters breakdown region. In this region, a large negative current will flow through the diode. Note that in breakdown both $v$ and $i$ (conventional directions) are negative.




There is a class of diodes called Zener diodes which are specially fabricated to operated in the breakdown region. These diodes are called Zener diodes. The breakdown voltage for Zener diodes is much smaller than 100 V. Zener diodes enter breakdown in the voltage range of $-18$ V to $-6$ V. Zener diodes behave exactly like real diodes in the forward-bias and reverse-bias regions.



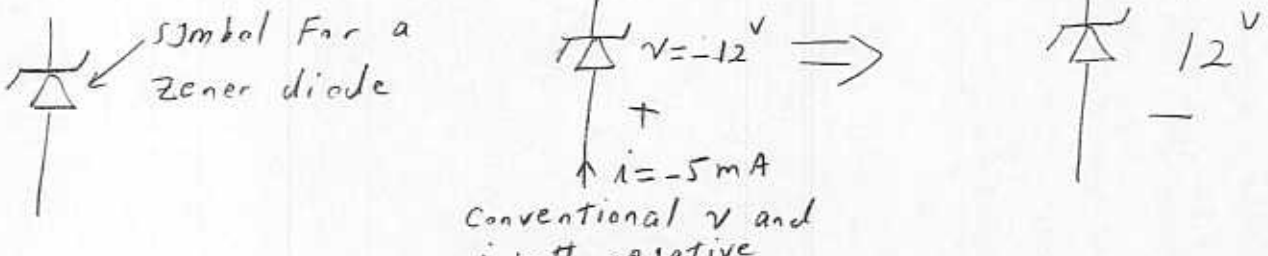



1) $V_{Zk}$ and $I_{Zk}$ are called the knee voltage and current. For currents and voltages above knee, the $i-v$ curve is almost a straight line.

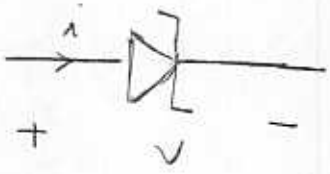
2) $V_{Z0}$ is the x-intercept of the linear portion of the $i-v$ curve.

3) $r_Z$ is the slope of the straight line that describes the $i-v$ curve beyond the knee point. $r_Z$ is called the incremental or dynamic resistance of the Zener diode.

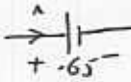
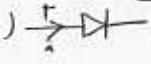
Ex. A Zener diode can have $V = -12^V$ and $i = -5^{mA}$ in the breakdown region (also called regulation region).

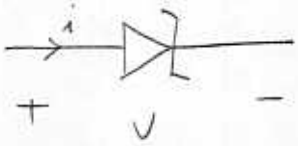


For a Zener diode operating in the regulation region, we prefer to use $i$ and $v$ conventions exactly opposite to the standard notation. This way we deal with positive current and voltage in breakdown. Note that if the Zener diode is operating in the Forward-bias (on) or reverse-bias (OFF) regions, we use the standard notation and the models discussed before.



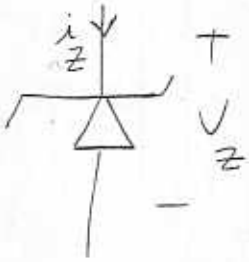
IF you assume on, we can use any of the four models discussed before

1)  2)  3)  4)  $i = I_s\left(e^{v/nV_T} - 1\right)$

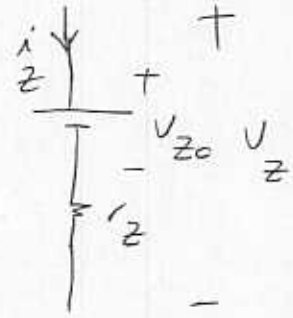


IF you assume OFF, replace the diode by an open circuit and verify $v < 0$ or $v < 0.7$ or $v < 0.65$ depending on the model you use.

Regulation or breakdown:

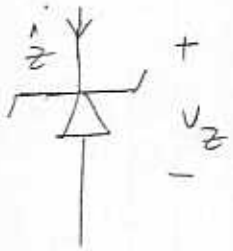


in regulation, the model is $\Rightarrow$

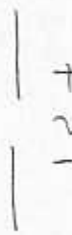


verify $i_z > 0$

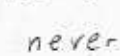
$$V_z = V_{z0} + r_z I_z$$

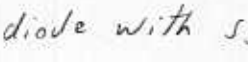


IF OFF, right before regulation

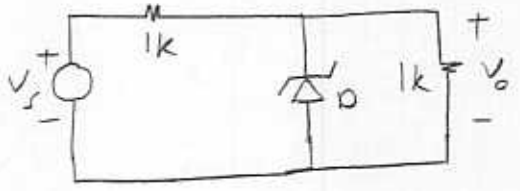


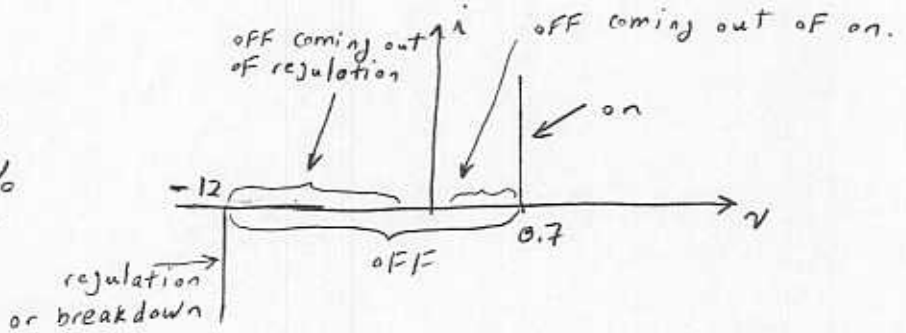
verify $v < V_{z0}$

Note that a diode with the symbol  is called a regular diode. A regular diode never operates in regulation because the voltage it requires for breakdown (about $-100^V$) is too large to supply. The diodes we have studied up to today are regular diodes that operate

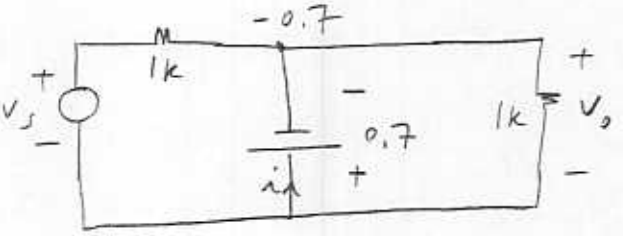
in Forward-bias or oFF region. A zener diode with symbol  is Fabricated to operate in breakdown. Zener diodes also act like regular diodes if forward-biased.

Ex. plot $V_o$ ⊥ $V_s$. Assume the diode is modeled by $V_{Z0} = 12^V$ and $r_z = 0\Omega$ in regulation and $V_D = 0.7^V$ in the Forward-biased region.




Assume on:



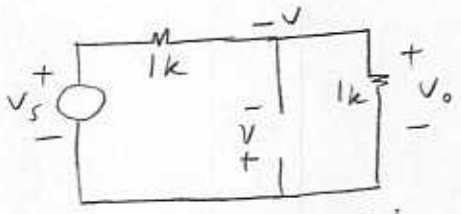

$\frac{-0.7-V_s}{1k} - i + \frac{-0.7}{1k} = 0 \Rightarrow i = \frac{-V_s-1.4}{1k} > 0$

$\Rightarrow V_s < -1.4$

if $V_s < -1.4 \Rightarrow$ D is on

KVL $\Rightarrow +0.7 + V_o = 0 \Rightarrow V_o = -0.7^V$

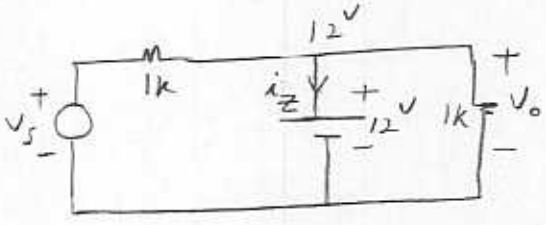
Assume oFF coming out oF on:




$\frac{-V-V_s}{1k} + \frac{-V}{1k} = 0 \Rightarrow V = -\frac{1}{2}V_s < 0.7 \Rightarrow V_s > -1.4$

if $V_s > -1.4 \Rightarrow$ D is oFF, $V_o = \frac{V_s}{2}$

Assume regulation:



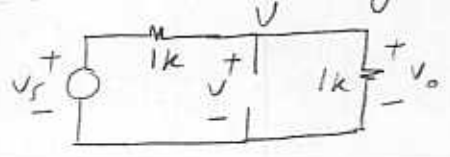

$\frac{12-V_s}{1k} + i_z + \frac{12}{1k} = 0 \Rightarrow i_z = \frac{V_s-24}{1k} > 0 \Rightarrow$

$V_s > 24$

if $V_s > 24 \Rightarrow$ D is in regulation

$V_o = 12^V$

Assume oFF coming out oF regulation



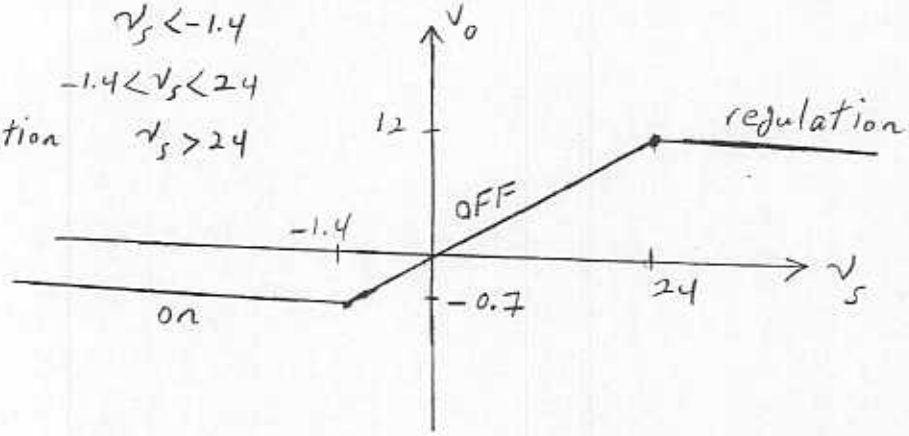

$\frac{V-V_s}{1k} + \frac{V}{1k} = 0 \Rightarrow V = \frac{1}{2}V_s < 12 \Rightarrow V_s < 24$

if $V_s < 24$, D is oFF and $V_o = \frac{V_s}{2}$

on $v_s < -1.4$

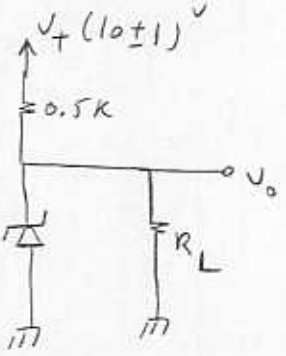
off $-1.4 < v_s < 24$

regulation $v_s > 24$



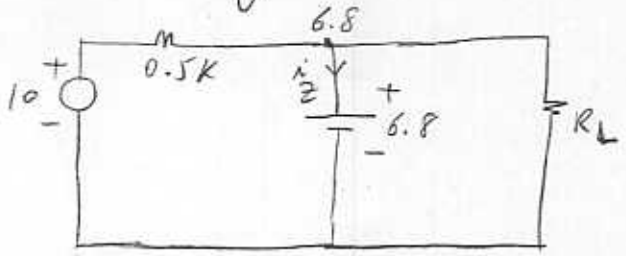

Note that a zener diode in regulation acts like a battery that can provide a constant voltage across a resistor.

Ex. Consider the circuit shown below with $V_{Z_0} = 6.8^V$ & $r_Z = 20^\Omega$.




a/ with $V_+$ equal to the nominal value of $10^V$, Find all values of $R_L$ for which the zener diode is operating in regulation.

Assume regulation: (For this part, we assume $r_Z = 0$).

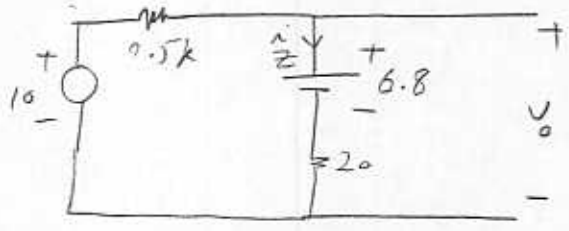



$$\frac{6.8-10}{0.5k} + i_Z + \frac{6.8}{R_L} = 0 \Rightarrow$$

$$i_Z = 6.4 \times 10^{-3} - \frac{6.8}{R_L} > 0 \Rightarrow R_L > 1.0625\,k$$

b/ Find the output voltage at no load ($R_L = \infty$).

Assume regulation:



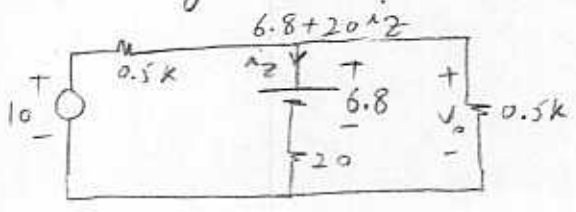

$$KVL \Rightarrow -10 + 0.5k\, i_Z + 6.8 + 20 i_Z = 0 \Rightarrow$$

$$i_Z = 6.15\,mA > 0 \checkmark$$

$$V_o = 6.8 + 20 i_Z = 6.923$$

c/ Find the output voltage when $R_L = 0.5k$

Assume regulation:

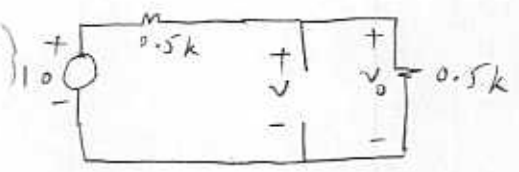



$$\frac{6.8 + 20 i_Z - 10}{0.5k} + i_Z + \frac{6.8 + 20 i_Z}{0.5k} = 0 \Rightarrow$$

$$i_Z = \frac{-3.6}{540} = -6.66\,m > 0 \times$$

Can not be in regulation

Assume OFF out of regulation:

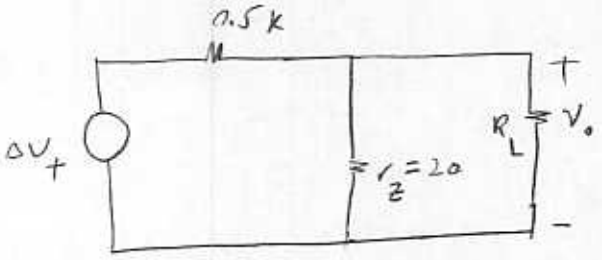



$$\frac{V-10}{0.5k} + \frac{V}{0.5k} = 0 \Rightarrow V = 5^V < 6.8^V \checkmark$$

$$V_o = V = 5^V$$

Notes: For $R_L > 1.0625\,k$, the load is kept at a constant voltage of about $6.8^V$ by the zener diode. The zener diode acts like a DC voltage supply of $6.8^V$ feeding the load $R_L$. This is the real application of a zener diode to maintain a constant voltage across a load.

Now, let's see how good of a DC voltage supply it is by finding how much its voltage change when the voltage supplied to the network by $V_+$ is changed from its nominal value of $10^V$ by $1^V$.




effective circuit to study changes about nominal values

$$\Delta V_o = \frac{20 \| R_L}{20 \| R_L + 0.5k} (\Delta V_+)$$

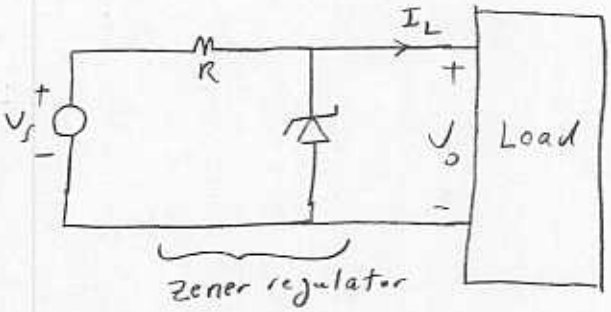
$$\simeq \frac{20}{20 + 0.5k} (\pm 1) = \pm 0.038^V$$

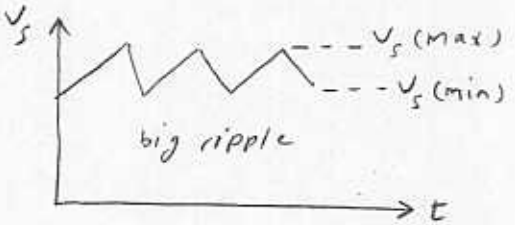
The voltage across the load changes by a very small amount ($0.038^V$) From the nominal value of $6.8^V$ when the input voltage changes unexpectedly by $1^V$. Hence, The zener diode is a very suitable DC voltage supply to the load.

# ENGR. 2364
## Handout #11

Applications of Zener diodes:

A Zener diode is used to provide a constant voltage with a very small ripple when the raw supply $V_s$ has a large ripple component. The Zener diode has to operate in regulation to provide an almost constant voltage of $V_o \cong V_{Z0}$. Note that the load $R_L$ is not specified in value. In a design problem, we are only given the range of values $I_L$ can take i.e., $I_L(min) \le I_L \le I_L(max)$.



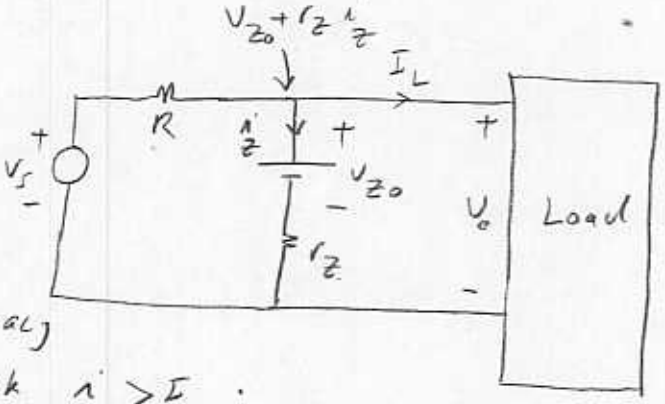


Let's Find $V_o$ in terms of $V_s$ with the Zener diode in regulation to see if $V_o$ has much smaller ripples than $V_s$.

Assume regulation:

$$\text{KCL} \Rightarrow \frac{V_{Z0} + r_Z i_Z - V_s}{R} + i_Z + I_L = 0 \Rightarrow$$

$$i_Z = \frac{V_s - V_{Z0} - R I_L}{R + r_Z} > 0 \quad \text{to verify regulation}$$




In real design problems, where accuracy is very important, we have to check $i_Z > I_{Zmin}$. $I_{Zmin}$, which is usually slightly bigger than $I_{Zk}$, would guarantee that the Zener diode is in breakdown. $i_Z > 0$ is fine for our every day problems. However, remember that in real life problems, we need $i_Z$ slightly greater than $i_{Zk}$ to make sure the Zener diode

is well into the breakdown region. In this design problem, we check $i_Z > I_Z(min)$ to make sure the zener diode satisfies this condition.

$$i_Z > I_Z(min) \Rightarrow \frac{V_S - V_{Z0} - R I_L}{R + r_Z} > I_Z(min) \Rightarrow \quad (1)$$

we can now find the required range of values of R to guarantee operation in regulation.

$$(1) \Rightarrow R < \frac{V_S - V_{Z0} - r_Z I_Z(min)}{I_L + I_Z(min)}$$

we need R less than the quantity on the right hand side to make sure the zener diode regulates in breakdown. Given that $V_S(min) \leq V_S \leq V_S(max)$ and $I_L(min) \leq I_L(max)$, we need

$$R < \frac{V_S(min) - V_{Z0} - r_Z I_Z(min)}{I_L(max) + I_Z(min)}.$$

This is to say that if $V_S(min)$ and $I_L(max)$ happen together at the same time, they result in the smallest value on the right hand side and R must remain smaller than this quantity for the zener diode to operate in breakdown.

$$R_{max}(allowed) = \frac{V_S(min) - V_{Z0} - r_Z I_Z(min)}{I_L(max) + I_Z(min)}$$

we can also solve for $V_o$ from the KCL equation on the previous page.

$$V_{Z0} + r_Z i_Z - V_S + R i_Z + R I_L = 0 \Rightarrow i_Z = \frac{V_S - V_{Z0} - R I_L}{R + r_Z}$$

$$V_o = V_{Z0} + r_Z i_Z = V_{Z0} \frac{R}{R + r_Z} + V_S \frac{r_Z}{R + r_Z} - I_L \frac{r_Z R}{r_Z + R} \quad (2)$$

Note that the ripples in input voltage $V_S$ propagate to the output

because $V_o$ depends on $V_s$.

$$V_o \propto V_s \frac{r_z}{R + r_z}$$

if $r_z << R$, then $\frac{r_z}{R + r_z}$ is very small. This means that $V_s$ or its ripples do not contribute much to the output.

Two parameters determine how well the regulator is performing its regulation.

$$\text{line regulation} = \frac{\Delta V_o}{\Delta V_s} = \frac{\text{change in } V_o}{\text{change in } V_s}$$

note that this quantity shows how input ripples ($\Delta V_s$) propagate to the output.

$$\text{load regulation} = \frac{\Delta V_o}{\Delta I_L} = \frac{\text{change in } V_o}{\text{change in } I_L}$$

note that this quantity shows how output voltage changes ($\Delta V_o$) with changes in load current ($\Delta I_L$).

For an ideal regulator, we want line and load regulations to be zero. We do not want ripples or changes in $V_s$ to change $V_o$ which is supposed to be a constant voltage feeding the load. This means an ideal line regulation of 0. Moreover, if $I_L$ changes, we do not want $V_o$ to change. $V_o$ is supposed to be a constant voltage feeding your load regardless of $I_L$ value.

From eq. 2 $\Rightarrow$ $\text{line regulation} = \frac{\Delta V_o}{\Delta V_s} = \frac{r_z}{R + r_z}$

$$\text{load regulation} = \frac{\Delta V_o}{\Delta I_L} = -(r_z \parallel R).$$

Ex. we need to supply an output voltage of $7.5^V$ to a load. The raw supply voltage varies between 15 and $25^V$. $I_L$ changes in the range 0 to 15 mA. The zener diode has $V_Z = 7.5^V$ when $I_Z = 20mA$ and its $r_Z = 10\Omega$. Find R, load and line regulations. Find the percentage change in $V_o$ corresponding to the full change in $V_s$ and the full change in $I_L$. Let $I_{Z(min)} = \frac{1}{3} I_{L(max)} = 5m$

solution:

$15 \le V_s \le 25$

$0 \le I_L \le 15^m$

Note that an operating point of the zener diode is specified.

$V_Z = 7.5^V$ when $I_Z = 20mA \Rightarrow$

$V_Z = V_{Z0} + r_Z I_Z \Rightarrow 7.5 = V_{Z0} + 10(20m) \Rightarrow V_{Z0} = 7.3^V$

Choose R to have its maximum value to get good line regulation.

$$R_{max\ (allowed)} = \frac{V_{s(min)} - V_{Z0} - r_Z I_{Z(min)}}{I_{L(max)} + I_{Z(min)}} = \frac{15 - 7.3 - 10(0.005)}{20 \times 10^{-3}} = 383\Omega$$

$$\text{line regulation} = \frac{r_Z}{R + r_Z} = \frac{10}{383+10} = 25.4 \times 10^{-3}$$

$$\text{load regulation} = -\frac{r_Z R}{r_Z + R} = -9.7$$

Full change in $V_s = \Delta V_s = 10 \Rightarrow 25.4 \times 10^{-3} = \frac{\Delta V_o}{\Delta V_s} = \frac{\Delta V_o}{10} \Rightarrow \Delta V_o = 0.254^V$

when $V_s$ changes by $10^V$, $V_o$ changes by 0.254. this means the voltage across the load remains fairly constant. The zener diode feeding the load is a good DC supply.

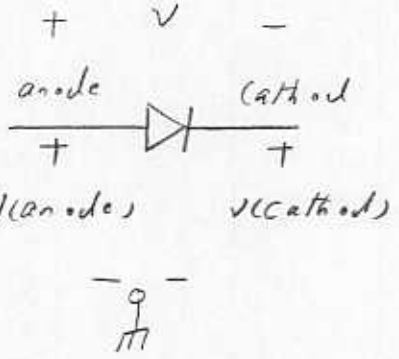
Full change in $I_L = 15mA \Rightarrow -9.7 = \frac{\Delta V_o}{\Delta I_L} = \frac{\Delta V_o}{15m} \Rightarrow \Delta V_o = -0.15^V$

A change in load current by 15 mA changes the output voltage by $-0.15^V$ only. Again the zener diode provides an almost constant voltage to the load [illegible]

ENGR. 2364
Handout #12

Peak detector:

In this handout, we assume the regular diode (not Zener diode) used is ideal. This means that when it is on, we model it by a short.



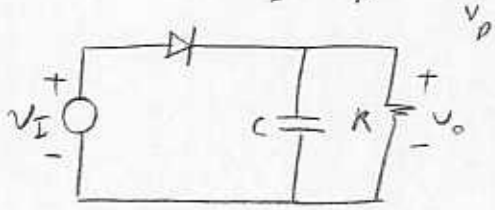

Note that For an ideal diode to turn on and become a short-circuit, anode must initially be at slightly higher voltage ($\epsilon$) compared to cathod. This makes $V = \epsilon$ a very small voltage that we always model by a short in on region.

$V = V(\text{anode}) - V(\text{cathod}) = \epsilon$

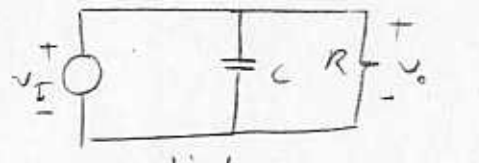
This means to turn the diode on, anode must initially become slightly higher in voltage than cathod.

Consider the circuit shown below.

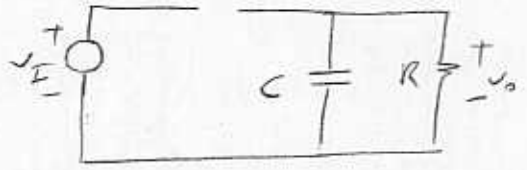
$v_I = V_p \sin 2\pi f t = V_p \sin \frac{2\pi}{T} t$

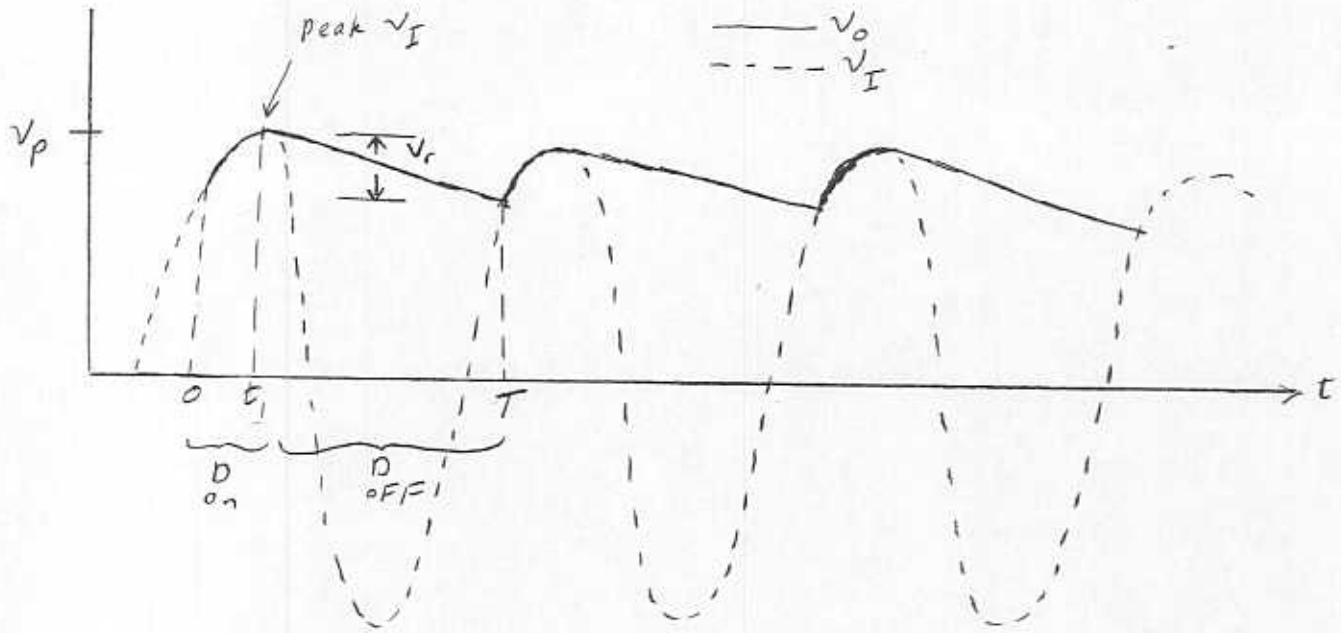



When $v_I$ becomes slightly higher than $v_o$, the diode turns on. Now, the voltage across the capacitor Follows the input voltage ($v_o = v_I$). Assume the diode turns on at time t=0 initially. we then have $v_c(t) = v_R(t) = v_o(t) = v_I(t)$ and the capacitor voltage charges up to the peak value of $v_I(t)$. Now, the cathod voltage is equal to anode voltage. At this peak value time $t_1$, the diode turns OFF because anode voltage is no longer slightly higher than cathod voltage.

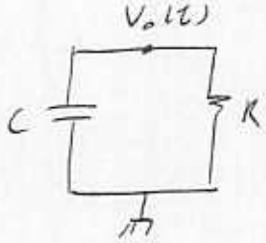



diode on
$v_o = v_I$






KCL $\Rightarrow C\frac{dV_o}{dt} + \frac{V_o}{R} = 0 \Rightarrow$




The solution to this differential equation is $V_o(t) = V_p e^{-(t-t_1)/RC}$.

This means for values of $t > t_1$, $V_o(t)$ decays because the exponent is negative.

At $t = T$, $V_I$ is increasing with time. $V_o$ is decreasing with time.

Anode voltage $V_I$ becomes slightly higher than cathod voltage $V_o$ and the diode turns on again and the whole process repeats itself.

The ripple voltage $V_r$ is defined as the difference between the minimum and maximum $V_o$. Note that T is the period of the sine wave.

$$V_o(t)\Big|_{max} = V_p \qquad V_o(t)\Big|_{min} = V_p e^{-(t-t_1)/RC}\Big|_{t=T} = V_p e^{-(T-t_1)/RC}$$

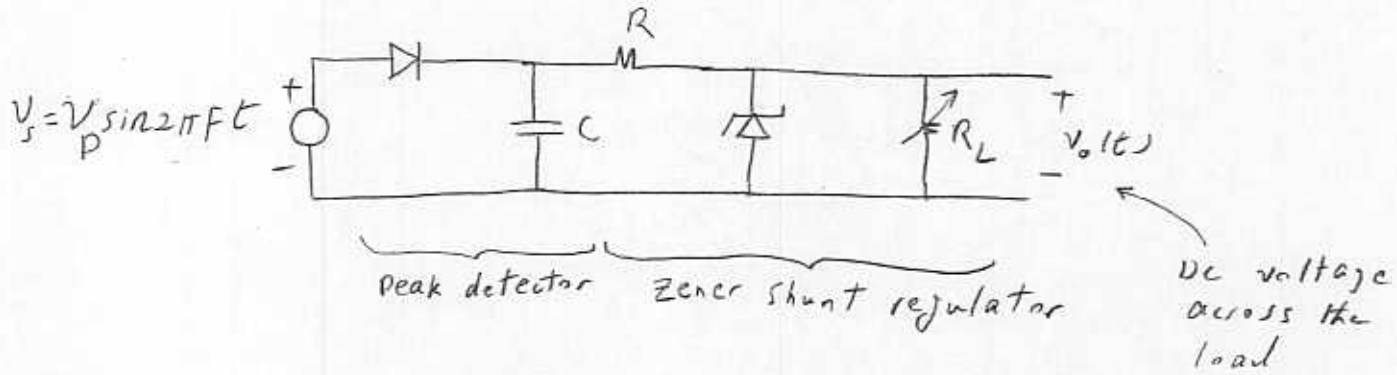
if $T \gg t_1 \Rightarrow V_o(t)\Big|_{min} \cong V_p e^{-T/RC}$

Now if $T \ll RC \Rightarrow e^{-T/RC} \cong 1 - \frac{T}{RC} \Rightarrow V_o(t)\Big|_{min} = V_p\left(1 - \frac{T}{RC}\right)$

$$V_r = V_o(t)\Big|_{max} - V_o(t)\Big|_{min} = V_p - V_p\left(1 - \frac{T}{RC}\right) = V_p\frac{T}{RC} = \frac{V_p}{fRC}$$

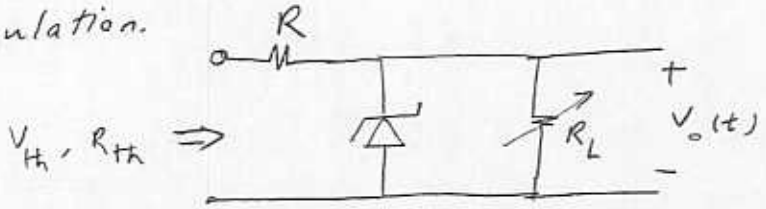
This is the ripple voltage in terms of $V_I(peak) = V_p$, frequency of $V_I$, R and C.

Design of a DC Power supply:




There are Two parts to this circuit, a zener regulator and a peak detector. Let's look at the zener regulator First.

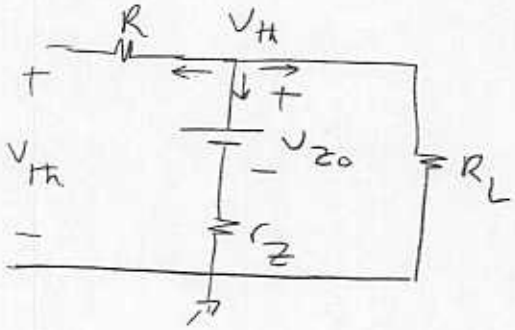
To have a DC supply, the zener diode must operate in regulation. Let's replace the zener diode by its regulation model and Then Find the Thevenin equivalent of the zener regulator.

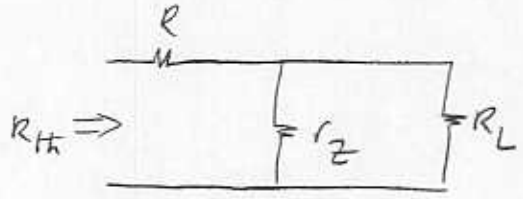



$$0 + \frac{V_{Th} - V_{Z0}}{r_Z} + \frac{V_{Th}}{R_L} = 0 \Rightarrow$$

$$V_{Th} = \frac{R_L}{R_L + r_Z} V_{Z0}$$

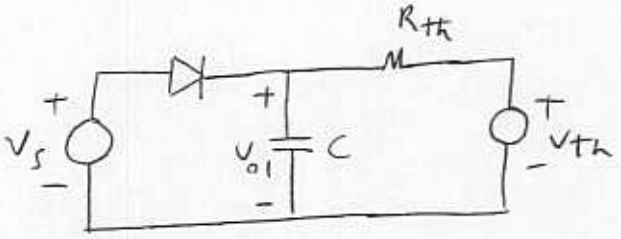
$$R_{Th} = r_Z \parallel R_L + R$$

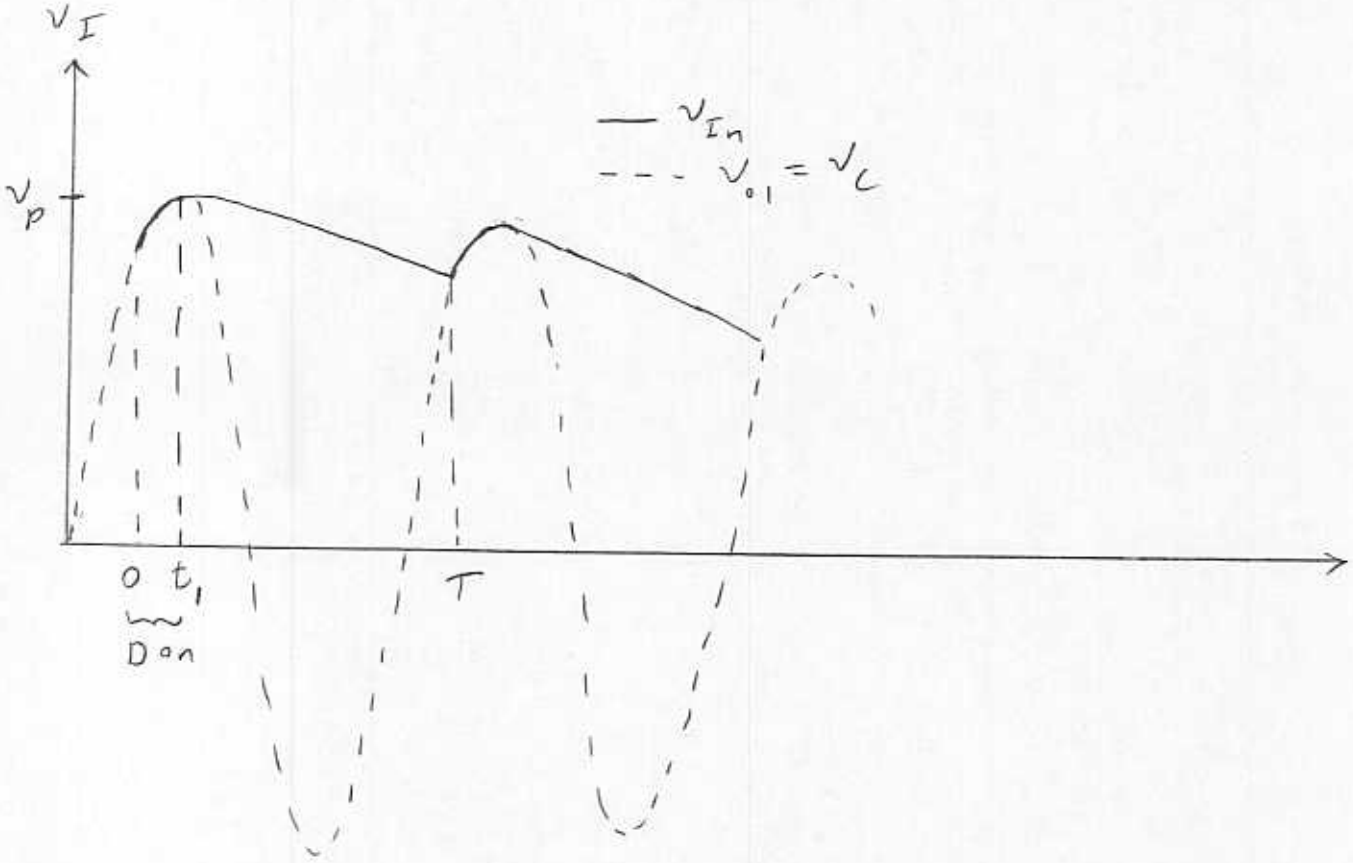


Now, let's study the peak detector with the Zener regulator replaced by its Thevenin equivalent

$V_I = V_p \sin 2\pi f t = V_p \sin \frac{2\pi}{T} t$

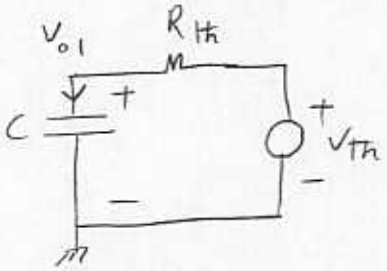



At $t=0$, the diode turns on again and stays on until $t = t_1$. After that, the diode goes off same as before

KCL $\Rightarrow C \frac{dV_{o1}}{dt} + \frac{V_{o1} - V_{th}}{R_{th}} = 0 \Rightarrow$ solution is

$V_{o1} = V_{th} + (V_p - V_{th})\, e^{-(t-t_1)/RC}$



what is the ripple voltage associated with $V_{o1}$.

$$V_{o1}\Big|_{max} = V_{o1}(t=t_1) = V_p$$

$$V_{o1}\Big|_{min} = V_{o1}(t=T) = V_{th} + (V_p - V_{th})\, e^{-(T-t_1)/RC}$$

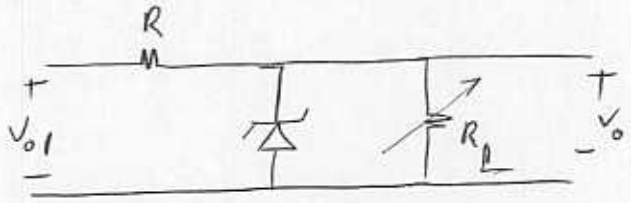
If $T >> RC \Rightarrow$ $V_{o1}\Big|_{min} = V_{th} + (V_p - V_{th})\left(1 - \frac{T}{RC}\right)$

$$V_{ro1} = V_{o1}\Big|_{max} - V_{o1}\Big|_{min} = \frac{T}{RC}(V_p - V_{th})$$

Now, we know the shape of the voltage across the capacitor ($V_{o1} = V_c$) and its ripple ($V_{ro1}$).

The Zener regulator, in effect, sees this voltage $V_{o1}$ as its input having a ripple of $V_{ro1}$.

The equations describing how $V_{o1}$ propagates to output and how the ripple in $V_{o1}$ propagate to the output were described before.



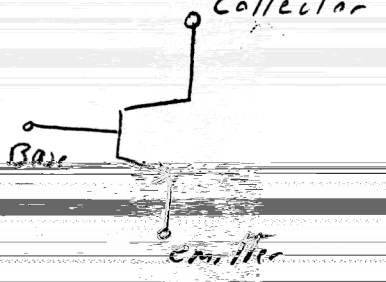

The rest of the problem is like doing the example on page 4 of handout # 11.

Handout #13

## Bipolar Junction Transistors (BJT):

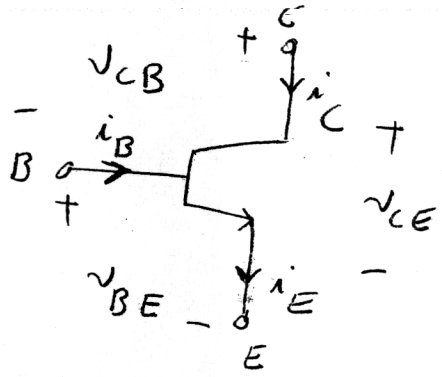
A BJT is a Three terminal device.

BJT Transistors are either pnp or npn.
We will Focus on npn transistors only.

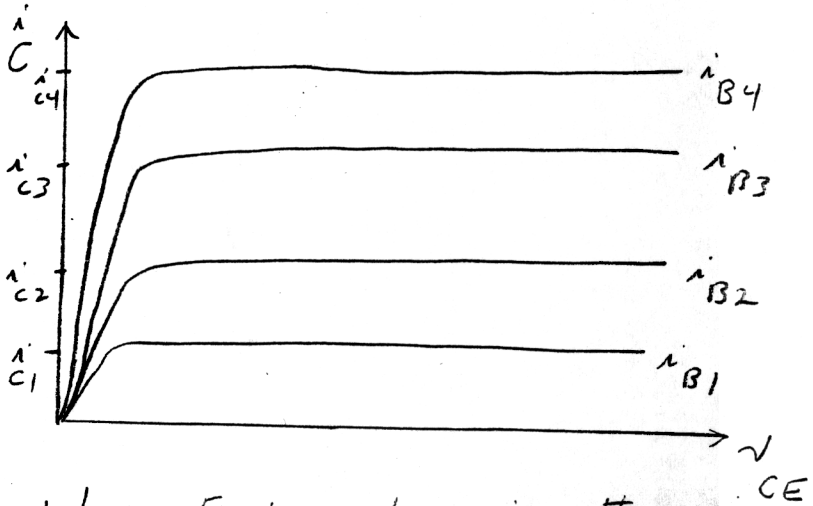



npn symbol

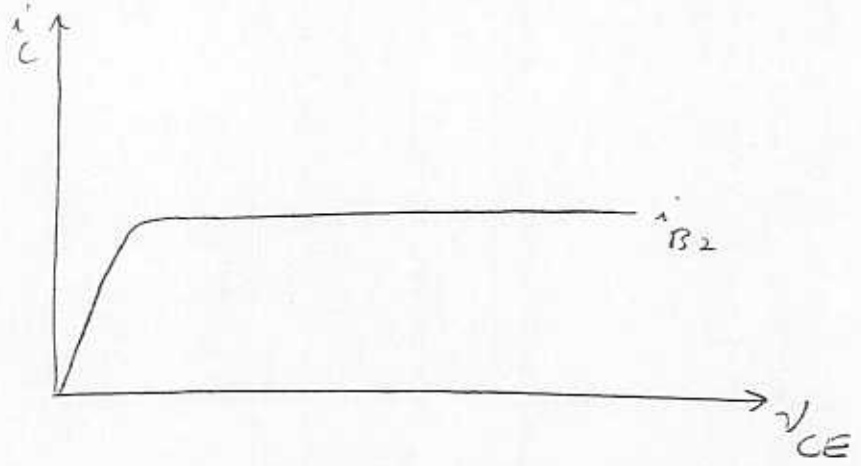
The currents and voltages of an npn transistor are shown below.



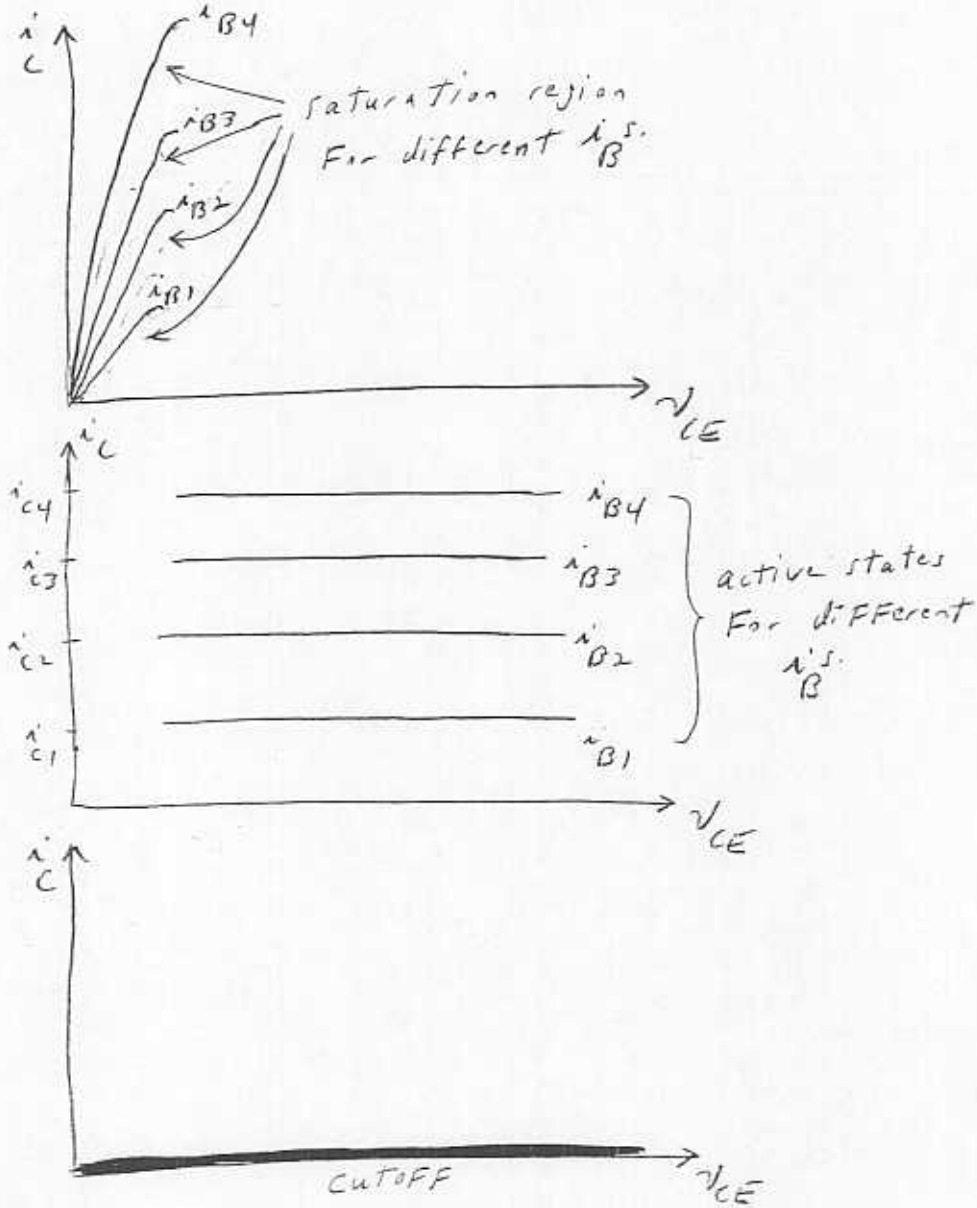

The i-v characteristic curve of an npn BJT is shown below.




Note that for a given value of $i_B$ such as $i_{B2}$, there is one curve that represents the i-v characteristic curve of the BJT.




A BJT has three regions of operation. These are called cutoff, active and saturation states. These regions of operation are shown below.




No matter what the state of operation of the BJT is, we have $i_E = i_B + i_C$

## Active state:

Note that in active state, the collector current $i_C$ does not change with $v_{CE}$. $i_C$ is flat in the active state. From the graph, it is clear that $i_C$ changes with $i_B$. In active state, we have

$$i_C = \beta i_B$$

$\beta$ is a parameter of the BJT which depends on the fabrication process and is specified by the manufacturer. Typically, we have $50 \leq \beta \leq 250$. A good transistor has a high value of $\beta$.

$$i_E = i_C + i_B = (\beta+1) i_B = (\beta+1)\frac{i_C}{\beta} \Rightarrow i_C = \frac{\beta}{\beta+1} i_E = \alpha i_E$$

$\alpha$ is another parameter which may be specified by the manufacturer. $\alpha$ has a value very close to one because $\beta$ is large.

In the active state, $i_C$ is related to $v_{BE}$ according to a diode i–v equation.

$$i_C = I_S e^{v_{BE}/V_T}$$

From this equation, it is clear that $i_C$ does not depend on $v_{CE}$

**Note:** In all the notations up to now, we have used the IEEE convention to represent currents and voltages.

Ex. $i_B$ = total base current which may have both DC & AC components

$v_{CE}$ = total voltage from collector to emitter which may have both DC & AC components.

$I_B$ = DC base current $\quad i_b$ = AC base current

$V_{CE}$ = DC voltage from collector to emitter

$v_{ce}$ = AC voltage from collector to emitter

IF a BJT is excited by DC supplies only, we use the notations $I_B$, $I_C$, $V_{BE}$, $V_{CE}$, .... to show that there are DC components only. IF a BJT is excited by DC+AC supplies, we use notations $i_B$, $i_C$, $v_{BE}$, $v_{CE}$, ... to show that both DC and AC components are present. The DC component is then represented by $I_B$, $I_C$, $V_{BE}$, $V_{CE}$, ... and the AC components by $i_b$, $i_c$, $v_{be}$, $v_{ce}$ ....

Note that $i_C = \beta i_B$ is a relationship between total base and collector currents. IF the BJT is only excited by DC supplies, we write

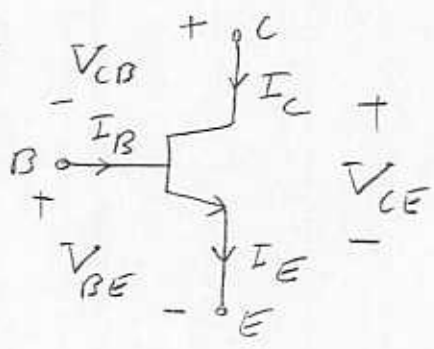
$$I_C = \beta I_B.$$

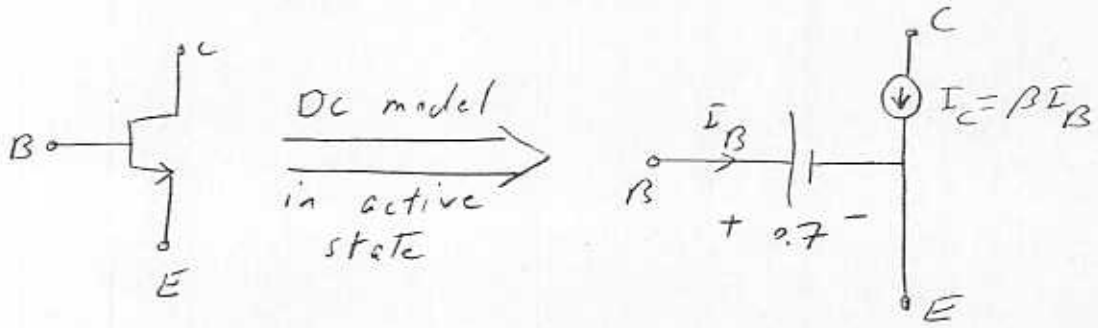
Similarly, $i_C = I_S e^{v_{BE}/V_T}$ is a relationship between the total base to emitter voltage and collector current. IF the BJT is only excited by DC supplies, we write

$$I_C = I_S e^{V_{BE}/V_T}.$$

Analysis of BJT circuits at DC:

When a BJT is operating in active state excited by DC supplies only, it effectively has a diode from base to emitter which is modeled by a constant battery of 0.7V. Note that this diode is on in active state. We also have $I_C = \beta I_B$ in active state.






$$I_E = (\beta+1) I_B$$

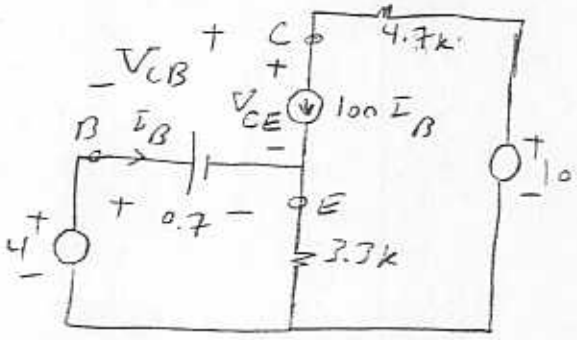
IF you assume a BJT is in active state, you have to verify your assumption at the end. we verify a BJT is on by showing

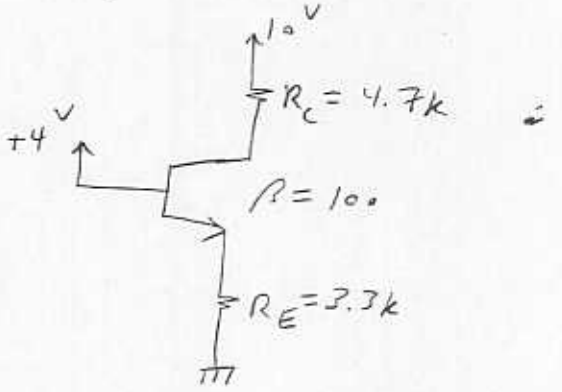
$$V_{CB} \geq 0 \quad \text{or} \quad V_{CE} > 0.2.$$

Either one of the inequalities shown above is sufficient to verify that the BJT is in active.

Ex. Find all currents and voltages of the BJT.

Assume active:




KVL $\Rightarrow -4 + 0.7 + 3.3k(101 I_B) = 0 \Rightarrow I_B = 0.0099\,mA \Rightarrow I_C = 100 I_B = 0.99\,mA$

$I_E = I_B + I_C = 101 I_B = 1mA$

KVL $\Rightarrow -10 + 4.7k(0.99m) + V_{CE} + 3.3k(1m) = 0 \Rightarrow V_{CE} = 2.047^V > 0.2$ ✓

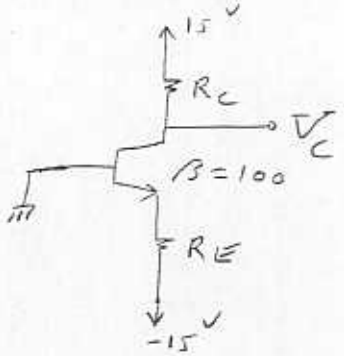
KVL $\Rightarrow -10 + 4.7k(0.99m) + V_{CB} + 4 = 0 \Rightarrow V_{CB} = 1.347 > 0$ ✓

Note that you only need to verify one inequality. You can choose which one.

Note that we can also get $V_{CB}$ from the following KVL.

$-V_{CE} + V_{CB} + V_{BE} = 0 \Rightarrow V_{CB} = 2.047 - 0.7 = 1.347^V$

Ex. The BJT shown has $V_{BE} = 0.7^V$ at $I_C = 1mA$.
Design the circuit to get $I_C = 2mA$ and $V_C = 5^V$



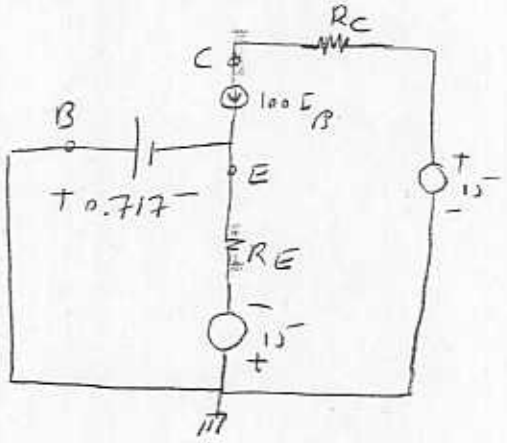

Solution: Assume the BJT is operating in active.

$$I_C = I_S e^{V_{BE}/V_T} \Rightarrow$$

$$\begin{cases} I_{C1} = I_S e^{V_{BE1}/V_T} \\ I_{C2} = I_S e^{V_{BE2}/V_T} \end{cases} \Rightarrow \frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \Rightarrow$$

$$V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{C2}} \Rightarrow V_{BE1} - 0.7 = 25\times10^{-3} \ln \frac{2m}{1m} \Rightarrow V_{BE1} = 0.717^V$$

For the BJT, we have $V_{BE1} = 0.717^V$, $V_C = 5^V$ and $I_C = 2mA$.




KVL $\Rightarrow -15 + R_C(2m) + V_C = 0 \Rightarrow$

$$R_C = \frac{15-5}{2m} = 5k$$

$$I_E = I_B + I_C = \frac{2}{100} + 2 = 2.02\,mA$$

KVL $\Rightarrow +0.717 + R_E(2.02m) - 15 = 0 \Rightarrow$

$$R_E = 7.07k$$

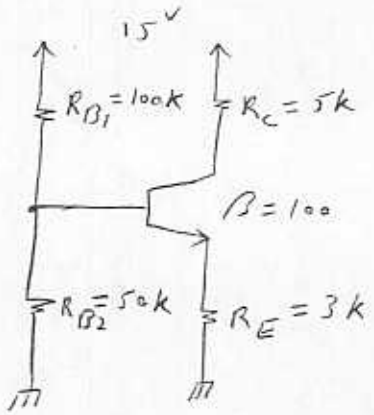
Design is complete because you have found unknowns $R_C$ and $R_E$ to give you $I_C = 2m$ and $V_C = 5^V$. You need to verify active state.

$$V_C = V_{CE} - 0.717 \Rightarrow V_{CE} = 5.717 > 0.2 \checkmark$$

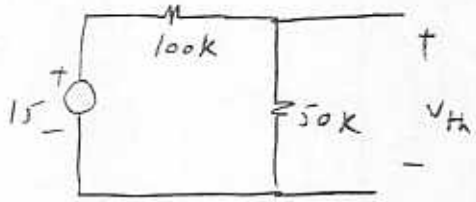
or $V_C = V_{CB} = 5^V > 0 \checkmark$

Ex. A standard BJT circuit:

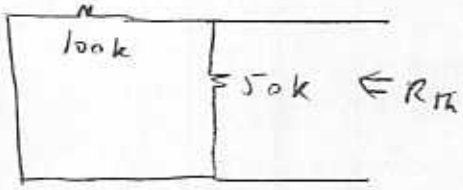
Find all voltages and currents of the BJT.



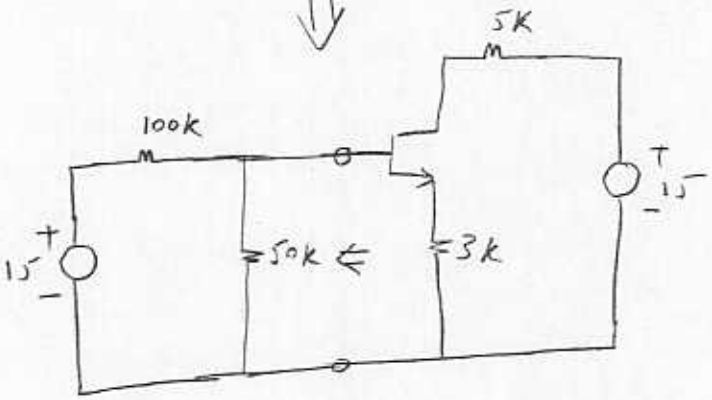

First apply Thevenin's Theorem to simplify the circuit.



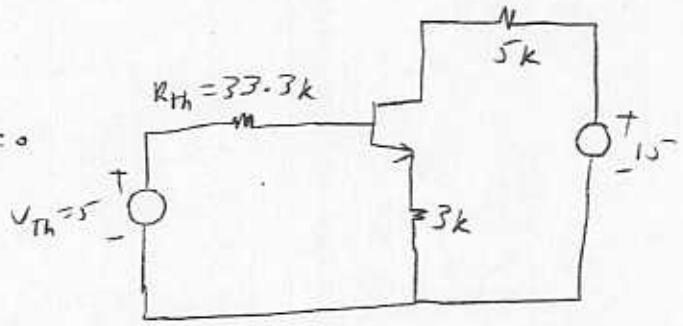

$$V_{th} = \frac{50k}{50k + 100k}(15) = 5^{V}$$




$$R_{th} = 100k \,||\, 50k = 33.3k$$




Assume active:




KVL $\Rightarrow -5 + 33.3k\, I_B + 0.7 + 3k(101\, I_B) = 0$

$\Rightarrow I_B = 0.0128\ mA$

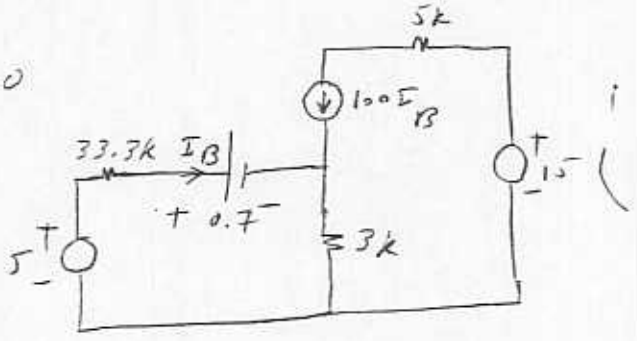
$I_C = 100\, I_B = 1.28\ mA$

$I_E = 101\, I_B = 1.29\ mA$

KVL $\Rightarrow -15 + 5k(1.28m) + V_{CE} + 3k(1.29m) = 0$

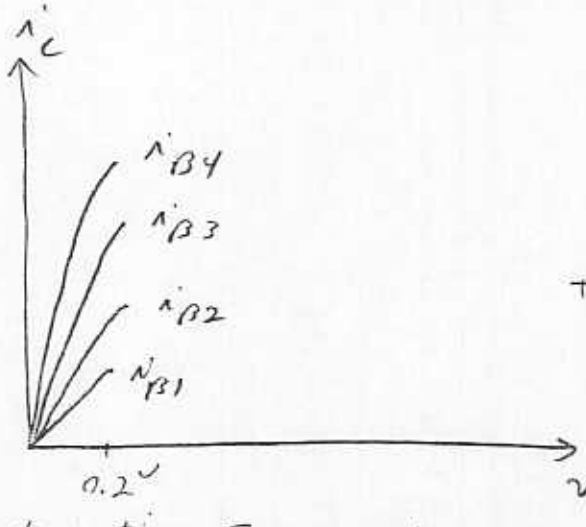
$\Rightarrow V_{CE} = 4.73^{V} > 0.2$ ✓

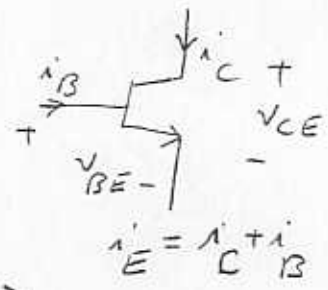
KVL $\Rightarrow V_{CE} = V_{CB} + 0.7 \Rightarrow V_{CB} = 4.03 > 0$ ✓



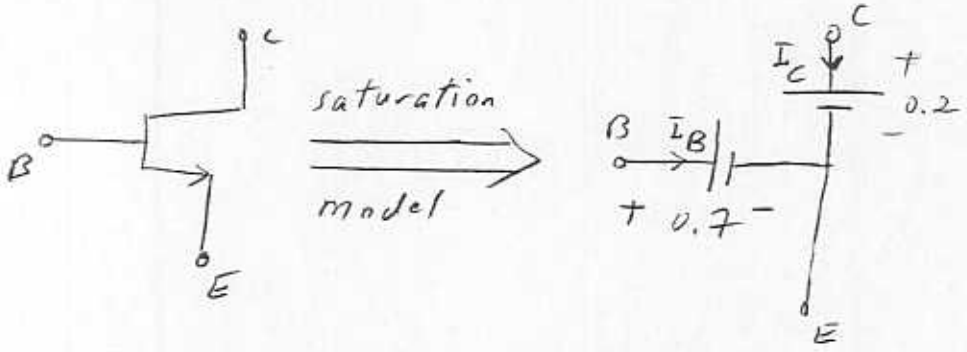
Saturation region:

Saturation region For a given base current is the region where $i_C$ varies linearly with $v_{CE}$.




Note that $v_{CE} \leq 0.2^V$ in saturation For any base current. It is a good approximation to take $v_{CE} = 0.2^V$ when the BJT is operating in saturation. In saturation, the base to emitter junction is still represented by a diode which is on. We model this diode by a constant battery of $0.7^V$.

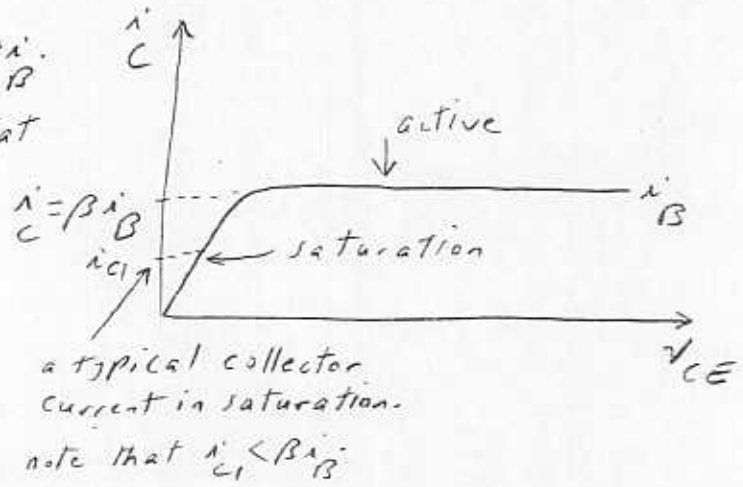



How do we verify saturation? Let's look at an $i$–$v$ curve For a given base current:

Note that in active state $i_C = \beta i_B$.

In saturation, any value of $i_C$ that you generate is below $\beta i_B$

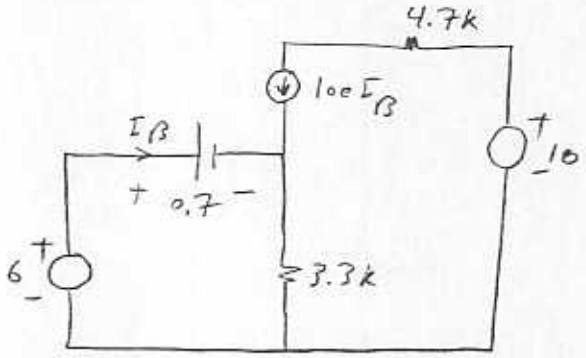
$\Rightarrow$ In saturation $i_C < \beta i_B$

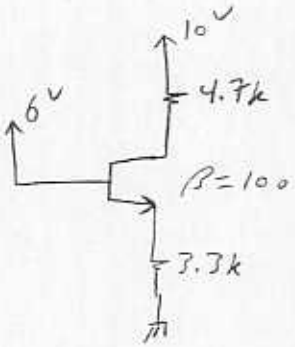


For a given base current, $i_C = \beta i_B$ is the maximum collector current the BJT can have. This happens in active state.

Ex. Find all voltages and currents of the BJT.

Assume active:




KVL $\Rightarrow -6 + 0.7 + 3.3k(101 I_B) = 0 \Rightarrow I_B = 0.0159\,mA$

$I_C = 100 I_B = 1.59\,mA$

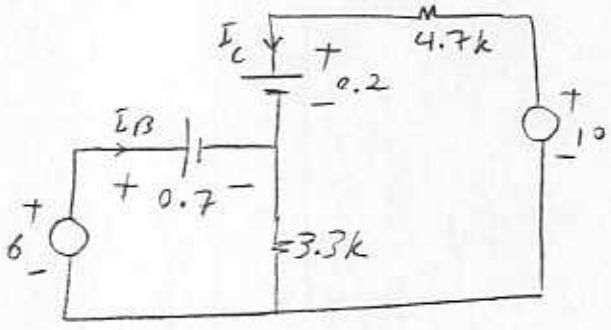
$I_E = I_C + I_B = 1.606\,mA$

KVL $\Rightarrow -10 + 4.7k(1.59m) + V_{CE} - 0.7 + 6 = 0 \Rightarrow V_{CE} = -2.773 > 0.2$ ✗

KVL $\Rightarrow V_{CB} = V_{CE} - 0.7 = -2.773 - 0.7 = -3.473 > 0$ ✗

BJT can not be in active.

Assume saturation:




KVL $\Rightarrow \begin{cases} -6 + 0.7 + 3.3k(I_B + I_C) = 0 \\ -10 + 4.7k I_C + 0.2 + 3.3k(I_B + I_C) = 0 \end{cases}$

$\Rightarrow I_B = 0.648m,\ I_C = 0.958\,mA$

verify assumption. Is $I_C < \beta I_B$.

$I_C = 0.958m < \beta I_B = 64.8mA$ ✓

$I_E = I_B + I_C = 1.606\,mA$

$V_{CE} = 0.2\,V$

KVL $\Rightarrow V_{CE} = V_{CB} + V_{BE} \Rightarrow$

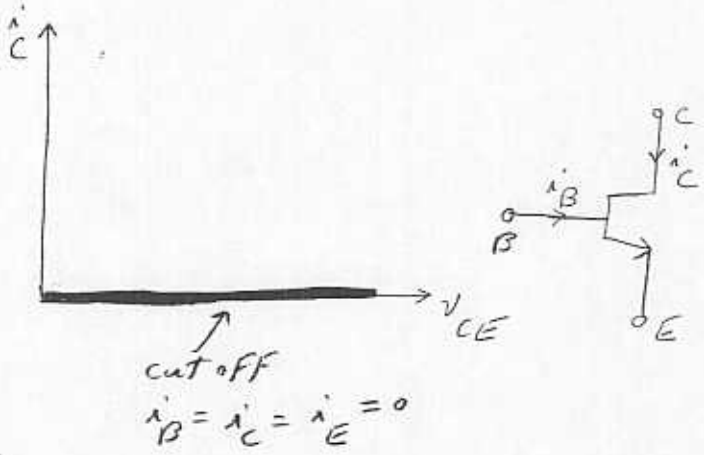
$V_{CB} = 0.2 - 0.7 = -0.5\,V$

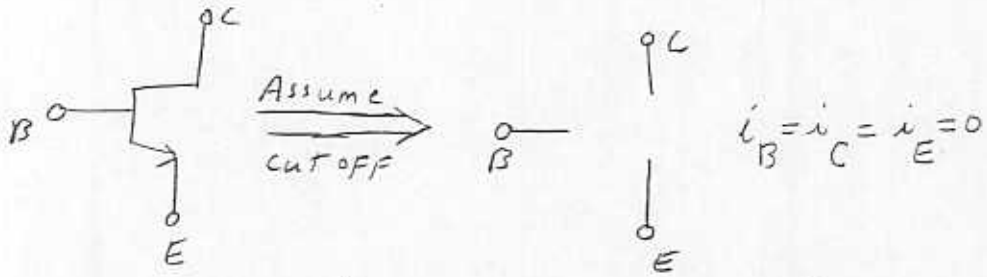
## Cut off:

In cut off, we have $i_B = i_C = i_E = 0$

In cut off, the diode at the base to emitter junction is reverse-biased. we model this diode by an open circuit.

To verify cut off, we check this diode being off through $V_{BE} < 0.7$ V.



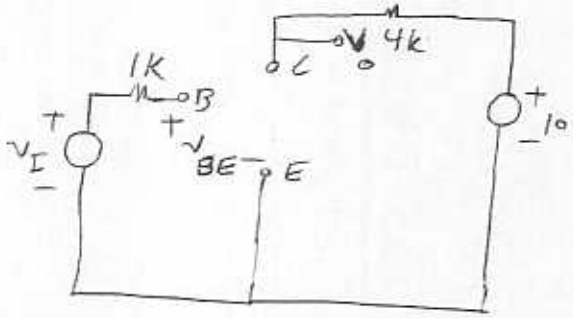



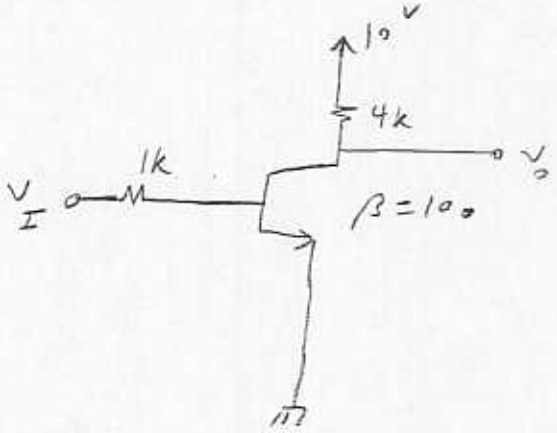

verify cut off by showing $V_{BE} < 0.7$.

In effect, when a BJT operates in cut off, we just take it out of the circuit.

Ex. plot $V_o \perp V_I$.

Assume cut off.

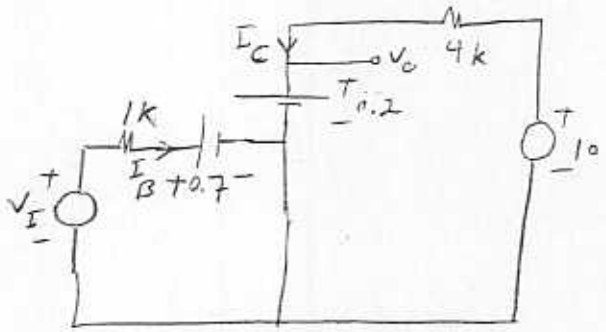



KVL $\Rightarrow -V_I + 1k\,(0) + V_{BE} = 0 \Rightarrow V_{BE} = V_I < 0.7$

As long as $V_I < 0.7 \Rightarrow$ BJT in cut off and $V_o = 10$ V.

Assume saturation:




$KVL \Rightarrow -V_I + 1k\, I_B + 0.7 = 0 \Rightarrow I_B = \frac{V_I - 0.7}{1k}$

$KVL \Rightarrow -10 + 4k\, I_C + 0.2 = 0 \Rightarrow I_C = 2.45mA$

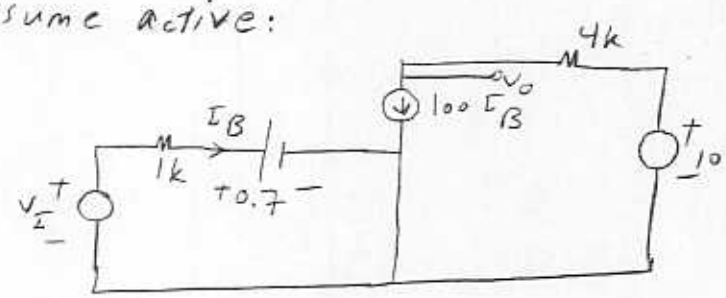
we need $I_C < \beta I_B \Rightarrow$

$2.45m < 100\, \frac{V_I - 0.7}{1k} \Rightarrow V_I > 0.7245^-$

$V_o = 0.2^V$

As long as $V_I > 0.7245 \Rightarrow$ BJT is in saturation and $V_o = 0.2^V$

Assume active:




$KVL \Rightarrow -V_I + 1k\, I_B + 0.7 = 0 \Rightarrow$

$I_B = \frac{V_I - 0.7}{1k}$

$I_C = 100\, I_B = \frac{100(V_I - 0.7)}{1k}$

$KVL \Rightarrow -10 + 4k\, \frac{100(V_I - 0.7)}{1k} + V_{CE} = 0 \Rightarrow$

$V_{CE} = 290 - 400 V_I > 0.2 \Rightarrow$

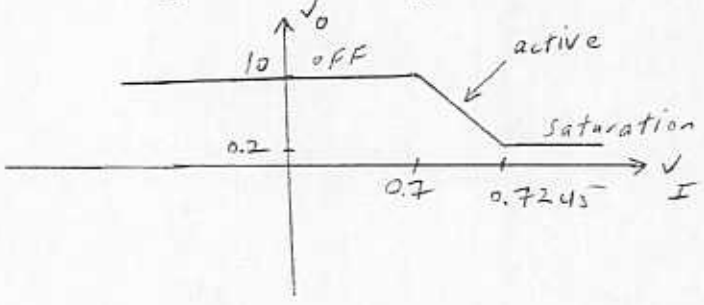
$V_I < 0.7245^-$

we also need $I_B > 0$ in active to show the base to emitter diode is on.

$I_B = \frac{V_I - 0.7}{1k} > 0 \Rightarrow V_I > 0.7$

As long as $0.7 < V_I < 0.7245$, the BJT is in active state and

$V_o = -4k\, I_C + 10 = -400 V_I + 280 + 10 = 290 - 400 V_I$




HMW: due Fri. Feb. 28th

4.3, 4.15 d, 4.20, 4.25, 4.26, 4.27, 4.28, 4.80,

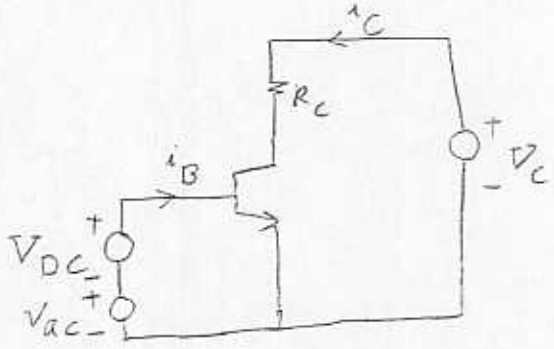
Sections covered: PP. 196–197 4.4, 4.6, PP. 267–276

ENGR. 364
Handout #15

Transistor as an amplifier:

In these applications, the BJT is excited with both DC and AC supplies. The DC supplies establish a DC operating point ($I_C$, $V_{CE}$). The DC operating point determines the AC model which is used to analyse the behavior of the BJT with AC supplies active. For a BJT to act as an amplifier for the AC input, it must be biased in the active state when only the DC supplies are present.

1) DC supplies are $V_C$ and $V_{DC}$
2) AC supply is $v_{ac}$




To Find the total (DC + AC) voltages and currents of the BJT, we first consider the DC circuit only. (superposition)

DC circuit:

To amplify any AC input, the BJT must be biased in the active state when DC supplies are present only.

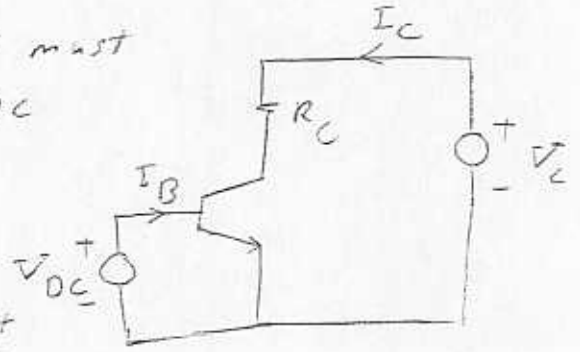
In active state, we have

$$I_C = I_S e^{V_{BE}/V_T}$$ (note that $V_{BE} = 0.7$ that we use in DC model is an approximation of this equation).

$$I_C = \beta I_B$$

$$-V_C + R_C I_C + V_{CE} = 0$$

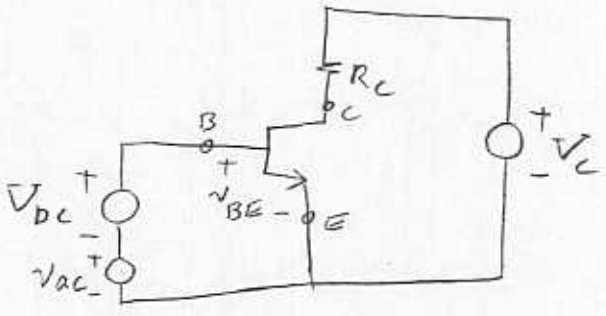
Need to verify $V_{CE} > 0.2$ or $V_{CB} > 0$.



Now, let's look at the operation of the circuit with both DC and AC supplies present.

$$v_{BE} = V_{BE} + v_{be}$$

we assume that $v_{be}$ (the AC portion of the base to emitter voltage) is so small that when added to $V_{BE}$, it does not take the BJT out of active state. we now have




$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T} = I_S e^{V_{BE}/V_T} e^{v_{be}/V_T} = I_C e^{v_{be}/V_T}$$

$$\Rightarrow i_C = I_C e^{v_{be}/V_T}$$

This is a relationship between the total collector current $i_C$, its DC component $I_C$ and the AC component of base to emitter voltage $v_{be}$

IF $v_{be} << V_T$ $\left(v_{be}\big|_{max} \leq 0.1\, V_T = 2.5\text{ mV at room temperature}\right) \Rightarrow$

$$i_C = I_C\left(1 + \frac{v_{be}}{V_T}\right) = I_C + \frac{I_C}{V_T} v_{be} \Rightarrow$$

$$i_C = I_C + i_c = I_C + \frac{I_C}{V_T} v_{be} \Rightarrow$$

$i_c$ = AC component of collector current $= \frac{I_C}{V_T} v_{be}$

This last equation shows how the AC collector current $i_c$ changes with the AC input $v_{be}$. It represents a relationship between AC quantities.

$$i_c = \frac{I_C}{V_T} v_{be} = g_m v_{be} \qquad g_m = \frac{I_C}{V_T} = \text{transconductance}$$

We also have

$$i_c = \beta i_B \Rightarrow i_B = \frac{i_c}{\beta} \Rightarrow$$

$$I_B + i_b = \frac{1}{\beta}(I_C + i_c) = \frac{I_C}{\beta} + \frac{1}{\beta} g_m v_{be} \Rightarrow$$

Since $I_B = \frac{I_C}{\beta}$ From the DC circuit $\Rightarrow$

$$i_b = \frac{g_m}{\beta} v_{be}$$

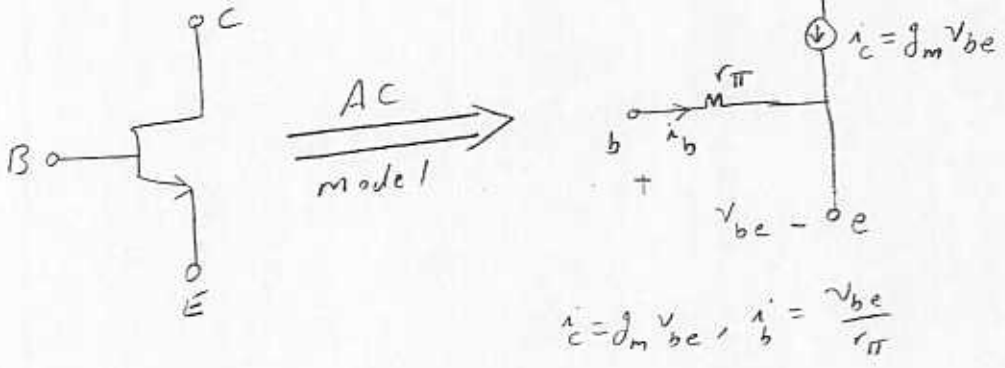
This is a relationship between the AC quantities $i_b$ and $v_{be}$

$$v_{be} = \frac{\beta}{g_m} i_b = r_\pi i_b \qquad r_\pi = \frac{\beta}{g_m}$$

The AC quantities $i_b$, $i_c$ and $v_{be}$ are related to each other through two equations.

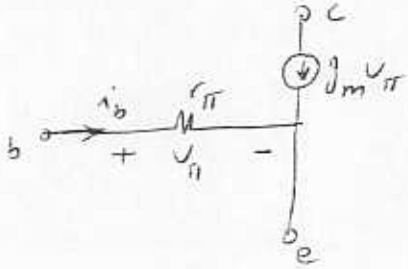
$$i_c = g_m v_{be} \quad \text{and} \quad v_{be} = r_\pi i_b$$

These two relationships define the AC model of the BJT which is used to study the effect of the AC supplies.




$$i_c = g_m v_{be}, \quad i_b = \frac{v_{be}}{r_\pi}$$

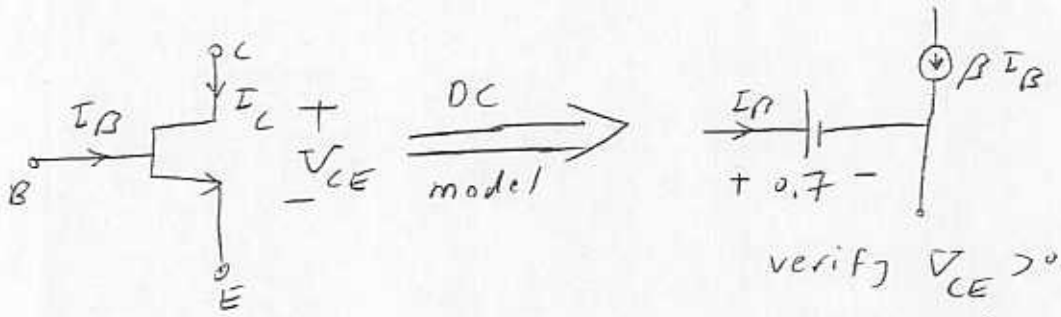
In some books, $v_{be}$ is also denoted as $v_\pi$.



Note that the AC model derived assumes $v_{be} \ll V_T \Rightarrow v_{be}\big|_{max} \leq 2.5mV$

In reality, we even let $v_{be}\big|_{max} = 10mV$. The AC model shown above is valid as long as $v_{be}$ stays below 10mV. This is called the small signal approximation For a BJT as an amplifier.

How do we solve a BJT amplifier problem?
We use superposition. First, we only consider the DC supplies and assume the BJT is in active. The model For BJT in active is



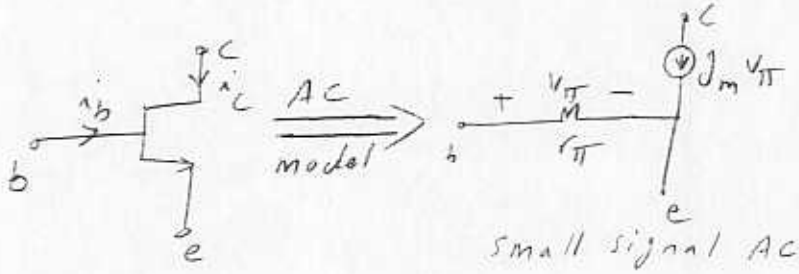

verify $V_{CE} > 0.2^V$
or $V_{CB} > 0$.

From the DC analysis, we obtain $I_C$ and $V_{CE}$. We can now Find the Parameters For the AC model.

$$g_m = \frac{I_C}{V_T}, \quad r_\pi = \frac{\beta}{g_m}$$

Note that these equations imply that the AC model of a BJT depends on the DC operating point $I_C$.

Now, we consider only the AC supplies. Replace the BJT with the AC model




Small signal AC model

From the AC analysis, we can find all the AC quantities such as $i_b$, $i_c$, $v_{be}$, $v_{ce}$ and so on. At this point, we need to verify $v_{be}|_{max} \leq 10mV$. If this condition is violated, the BJT model for AC analysis is not valid!

Now, according to superposition, we can add the DC and AC components of all voltages and currents to get the total (DC+AC) signals

$$i_C = I_C + i_c$$
$$i_B = I_B + i_b$$
$$v_{CE} = V_{CE} + v_{ce}$$
$$v_{BE} = V_{BE} + v_{be}$$

and so on.

# ENGR. 364

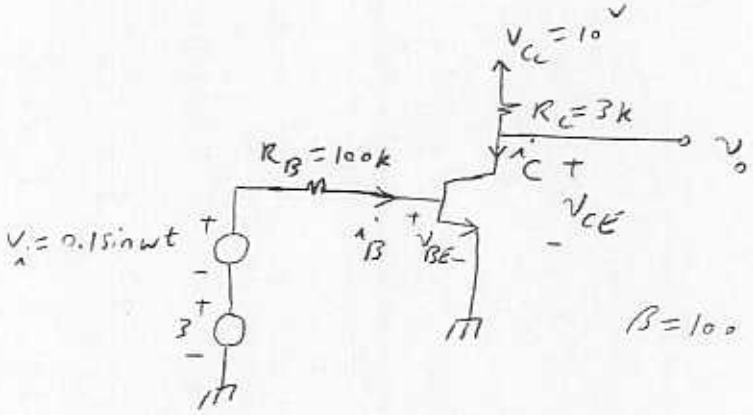
## Handout # 16

BJT as amplifier:

EX. #1 (Common-emitter amplifier):

Find $i_B$, $i_C$, $v_{BE}$ and $v_{CE}$

Also Find the AC voltage gain $\frac{v_o}{v_{be}}$




(A) DC analysis: (Assume BJT in active)

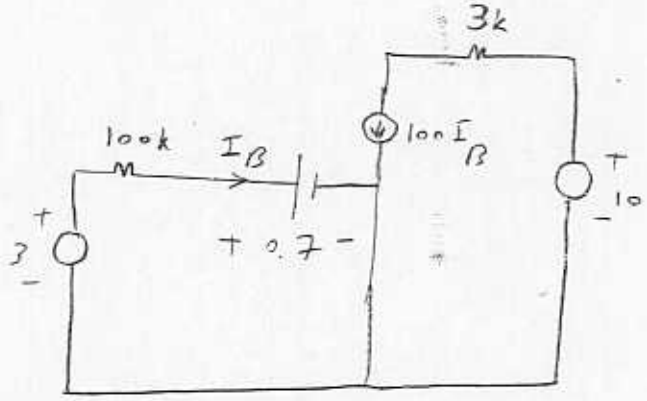
kill AC supplies

$-3+100k\,I_B+0.7=0 \Rightarrow I_B=0.023mA$

$I_C=100\,I_B=2.3mA$

$-10+3k(2.3m)+V_{CE}=0 \Rightarrow$

$V_{CE}=3.1\,V > 0.2$ ✓




$g_m=\frac{I_C}{V_T}=\frac{2.3m}{25m}=0.092\,\mho$

$r_\pi=\frac{\beta}{g_m}=\frac{100}{0.092}=1.09k$

DC voltages and currents:

$I_B=0.023mA,\ I_C=2.3mA,\ V_{BE}=0.7\,V,\ V_{CE}=3.1\,V$

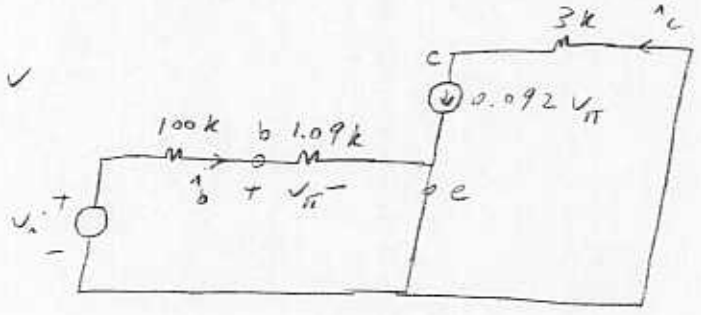
(B) AC analysis (kill DC supplies):

KVL $\Rightarrow i_b=\frac{v_i}{101.09k}\cong 0.001\sin\omega t\ mA$

$v_{be}=v_\pi=\frac{1.09k}{100k+1.09k}v_i=0.001\sin\omega t\ V$

$i_c=0.092\,v_\pi=0.092\sin\omega t\ mA$

KVL $\Rightarrow 3k(0.092\sin\omega t\ m)+v_{ce}=0 \Rightarrow$



$v_{ce} = -0.276 \sin \omega t$

verify small signal model is valid:

$$v_{be}\Big|_{max} = v_{\pi}\Big|_{max} = 0.001\ V = 1\ mV < 10\ mV \checkmark$$

Now From superposition, we can Find the total (DC+AC) signals.

$i_B = I_B + i_b = 0.023 + 0.001 \sin \omega t \ mA$

$i_C = I_C + i_c = 2.3 + 0.092 \sin \omega t \ mA$

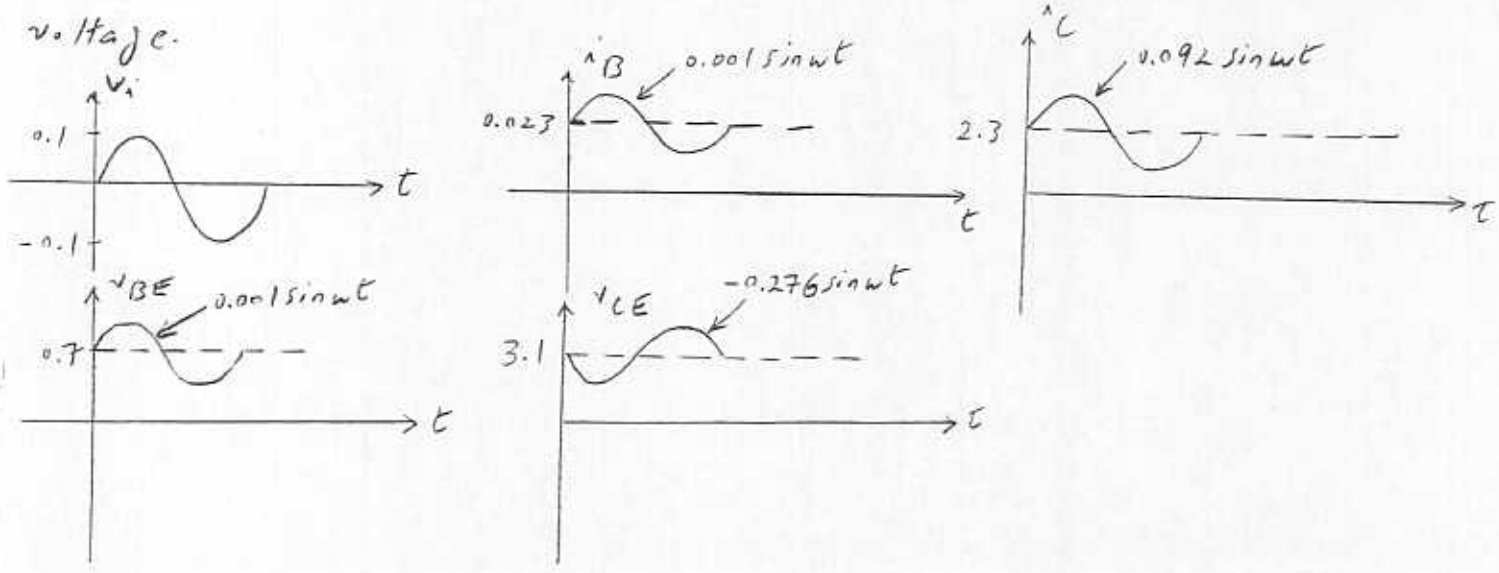
$v_{BE} = V_{BE} + v_{be} = 0.7 + 0.001 \sin \omega t \ V$

$v_{CE} = 3.1 - 0.276 \sin \omega t \ V$

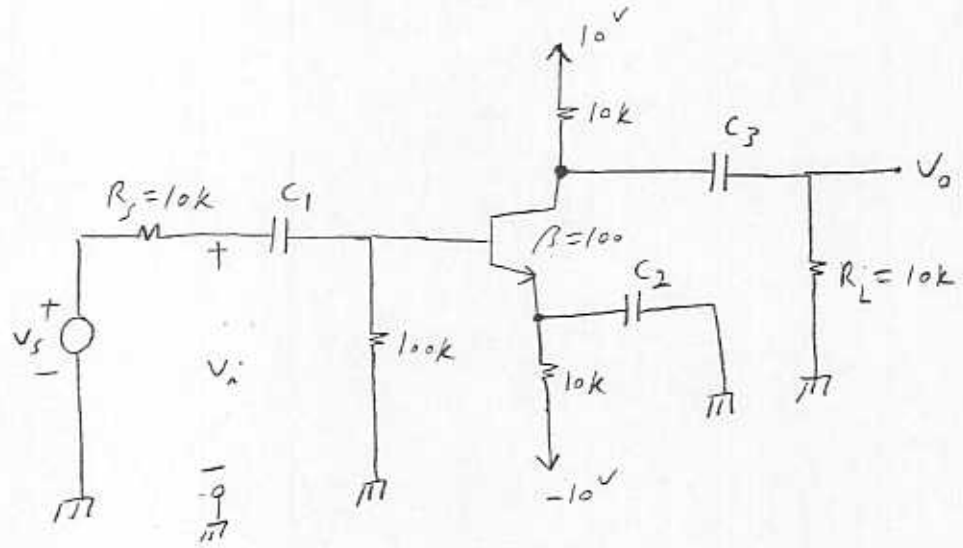
Note that $v_{be}(max) = 0.001$ is 700 times smaller than $V_{BE}$. Hence, it does not take the BJT biased in the active region using the DC supplies out of active state.

$$gain = \frac{v_o(AC)}{v_{be}} = \frac{v_{ce}}{v_{be}} = \frac{-0.276 \sin \omega t}{0.001 \sin \omega t} = -276$$

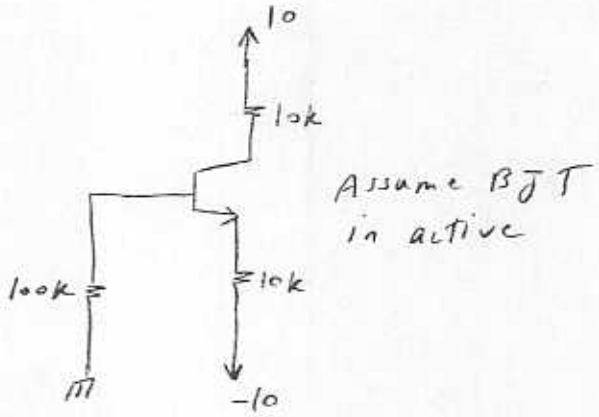
$v_i$ Feeds the base to emitter voltage of the BJT by the amount $v_{be}$. This voltage is amplified at the collector of the BJT by a Factor of 276. Therefore, the BJT is amplifying its base to emitter voltage.

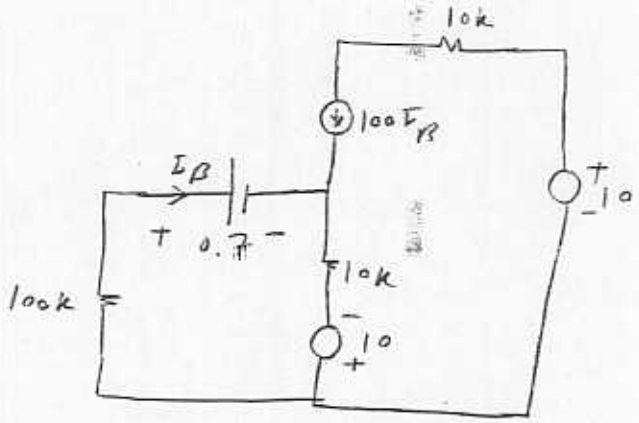


The common-emitter amplifier: (General Form)




(A) DC Analysis (kill AC supplies, open capacitors)




KVL $\Rightarrow$ $100k I_B + 0.7 + 10k(101 I_B) - 10 = 0 \Rightarrow I_B = 0.0084\ mA$

$I_C = 100 I_B = 0.84\ mA$

KVL $\Rightarrow$ $-10 + 10k(0.84m) + V_{CE} - 0.7 - 100k(0.0084m) = 0 \Rightarrow V_{CE} = 3.14^V > 0.2$ ✓

$g_m = \frac{I_C}{V_T} = \frac{0.84}{25} = 0.0336\ \mho$

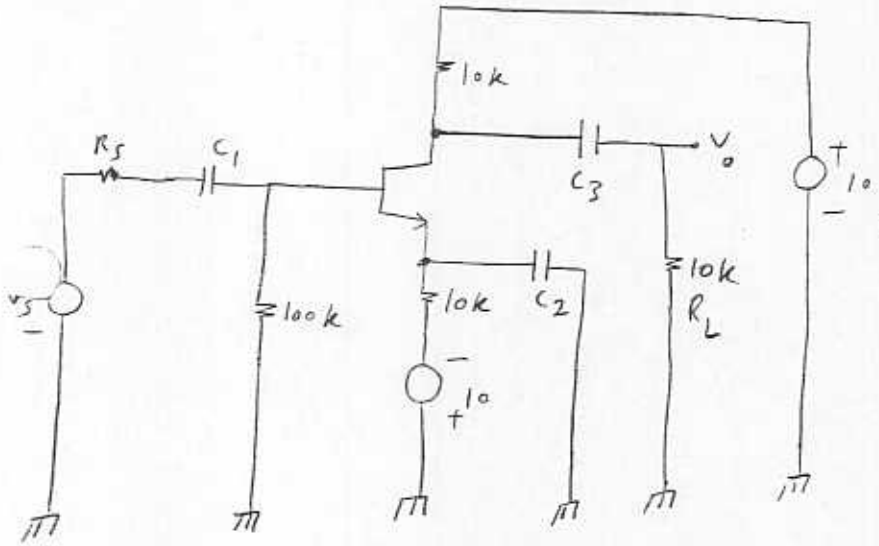
$r_\pi = \beta / g_m \cong 3k$

AC Analysis (kill DC supplies, short capacitors):

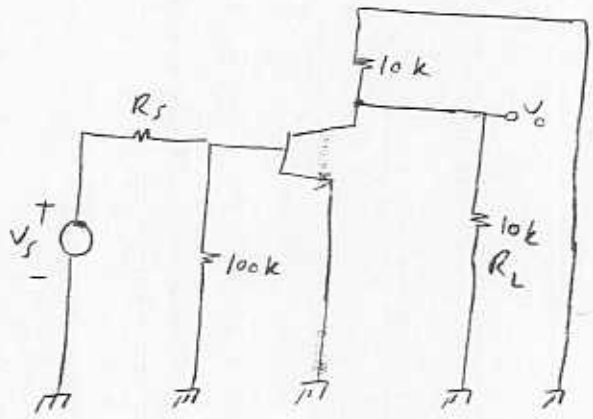
Note that For a sinusoidal input, the impedance of a capacitor is given by $\frac{-j}{\omega C} = -\frac{j}{2\pi f C}$ where $f$ is the frequency of $V_s$. We assume that the frequency of $V_s$ is chosen such that

$$-\frac{j}{2\pi f C} \longrightarrow 0.$$

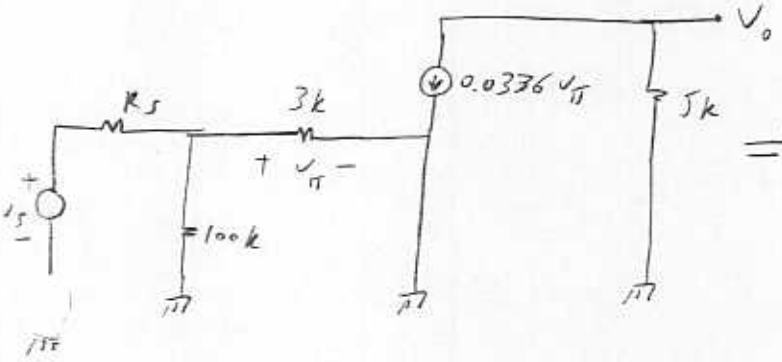
This means that we can replace all capacitors by short-circuits in the AC circuit.

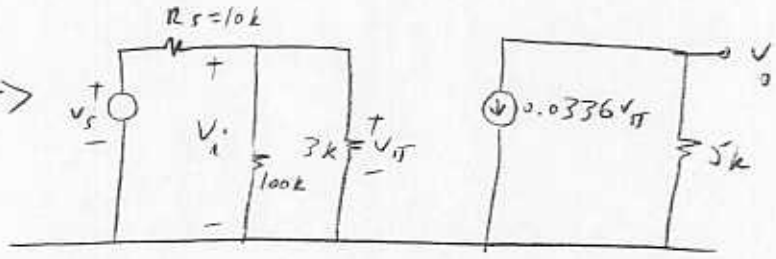



The entire circuit with both DC and AC supplies

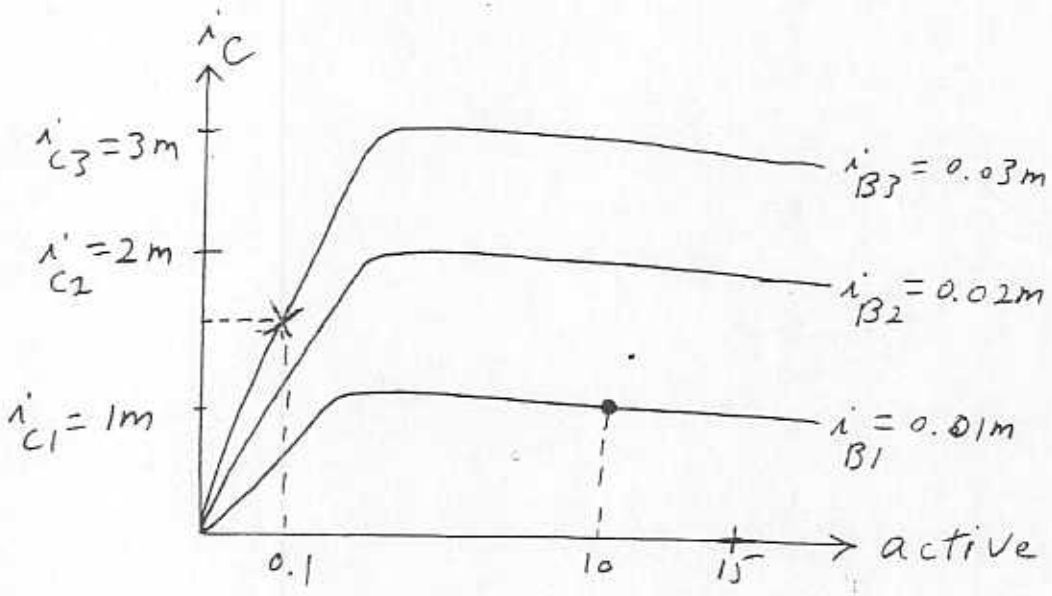



AC circuit
kill DC supplies
short capacitors



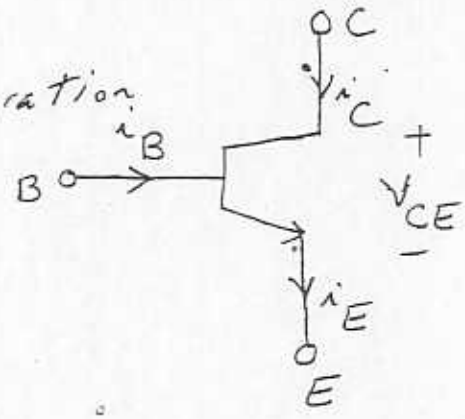
Ex.




$i_B = 0.01m$, $i_C = 1m$, $V_{CE} = 10^V$ • active

$i_B = 0.03m$, $i_C = 1.5m$, $V_{CE} = 0.1$ X saturation

$i_B = 0$, $i_C = 0$, $V_{CE} = 15^V$ + cutoff



quantities of interest are

① $v_o/v_i = v_o/v_\pi$. This is the amplifier gain from $v_{be}$ to $v_o$.

$v_o = -5k(0.0336 v_\pi) \Rightarrow v_o/v_\pi = -168$

② $v_o/v_s$ This is the overall gain.

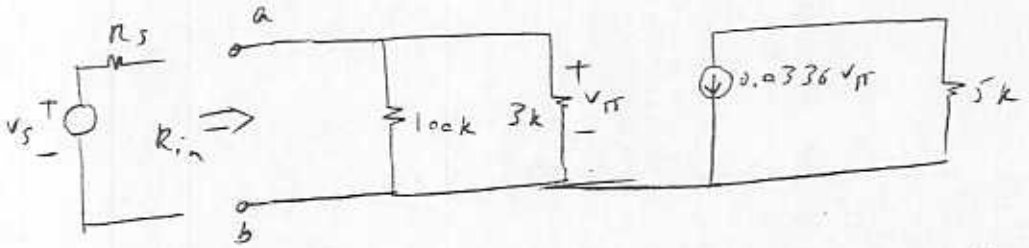
$v_o = -5k(0.0336 v_\pi)$

$$v_\pi = \frac{3k \,//\, 100k}{3k \,//\, 100k + 10k} v_s = 0.2248 v_s$$

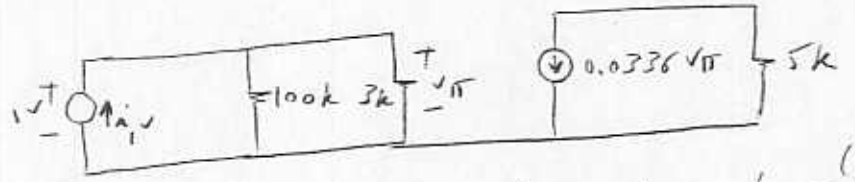
$$\frac{v_o}{v_s} = \frac{v_o}{v_\pi}\frac{v_\pi}{v_s} = -5k(0.0336)(0.2248) = -37.76$$

This amplifier amplifies $v_s$ by a factor of 37.76.

③ In this problem, the combination of $v_s$ and $R_s$ represent the AC power supply feeding the BJT. One quantity of interest is $R_{in}$ which is the equivalent resistance seen by the power supply when connected to the BJT.



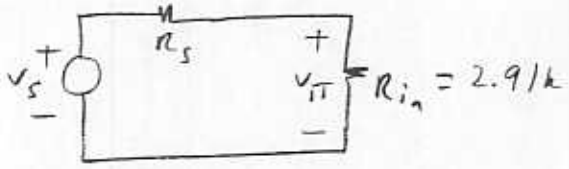

To Find $R_{in}$, apply a $1^V$ power supply between a and b. Find the current through the $1^V$ supply. Then $R_{in} = \frac{1^V}{i_{1V}}$.



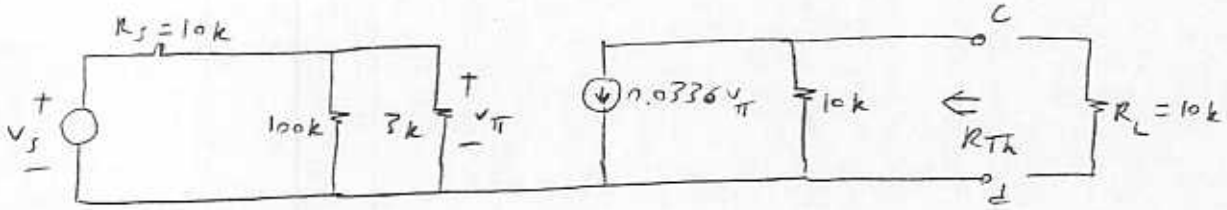

KCL $\Rightarrow -i_{1V} + \frac{1}{100k} + \frac{1}{3k} = 0 \Rightarrow i_{1V} = \frac{1}{100k} + \frac{1}{3k} \Rightarrow R_{in} = \frac{1}{i_{1V}} = \frac{(100k)(3k)}{100k+3k}$

$\Rightarrow R_{in} = 3k \,//\, 100k = 2.91k$

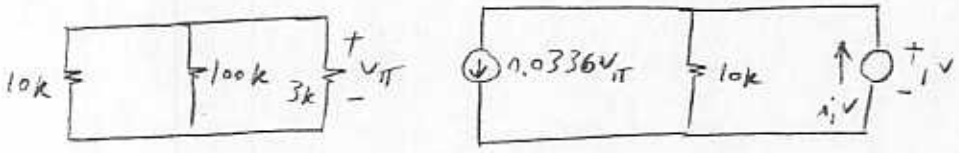
$R_{in}$ has the significance that it can be connected to the power supply $V_s$ and $R_s$. The power supply can not tell whether it is connected to just $R_{in}$ or the BJT amplifier. The two are equivalent in terms of what they do to the power supply $V_s$ and $R_s$.




(4) Another quantity of interest is $R_{th}$ or $R_{out}$ excluding $R_L$.



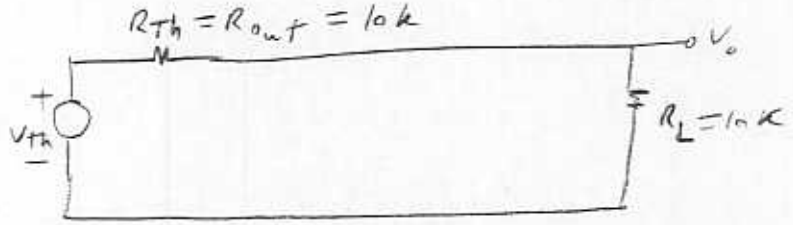

To Find $R_{th}$, kill the independent AC supply $V_s$. Apply a 1V supply between c and d. Find $i_1'$. Then $R_{th} = \frac{1}{i_1'}$.




KCL $\Rightarrow \frac{V_\pi}{10k} + \frac{V_\pi}{100k} + \frac{V_\pi}{3k} = 0 \Rightarrow V_\pi = 0$

KCL $\Rightarrow 0.0336 V_\pi + \frac{1}{10k} - i_1' = 0 \Rightarrow i_1' = \frac{1}{10k} \Rightarrow R_{Th} = \frac{1}{i_1'} = 10k$

We can draw an equivalent circuit for the BJT amplifier.



The entire BJT circuit excluding $R_L$ can be represented by $V_{th}$ and $R_{th}$. $R_L$ can not tell whether it is connected to the BJT amplifier or just $V_{th}$ and $R_{th}$. Note that

$$V_o = \frac{R_L}{R_L + R_{out}} V_{th}$$

Comparing the values of $R_L$ and $R_{out}$ determines how big $V_o$ (output voltage) is. If $R_{out} >> R_L$, then $V_o$ will be very small. This means that most of the voltage provided by the BJT amplifier is consumed by $R_{th}$ which represents the BJT amplifier. $R_L$, on the other hand, which is the output load gets a very small voltage. Having $R_{out} >> R_L$ is a bad design. In effect, you have designed a voltage amplifier that does not feed a significant voltage to its load and takes most of the voltage internally. This is to say that $R_{out}$ representing the amplifier doesn't deliver a significant voltage.

HMW: (due Wed. March 5th):

4.58, 4.62 (in part c, ignore $r_o$), 4.64, 4.65 (in part b, ignore T model)

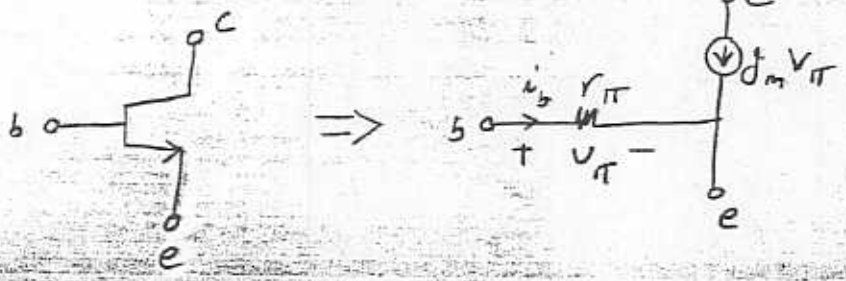
4.69, 4.71,

(7) For the Figures P4.78 and P4.80, Find $R_B$ For saturation.
let $\beta = 100$.

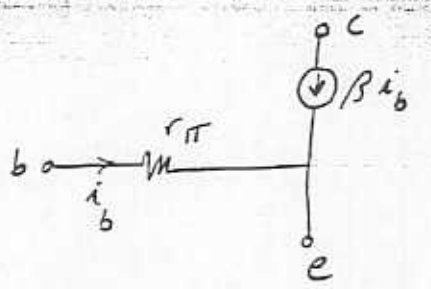
Sections covered From ch.4
4.7, 4.8

# Handout #16

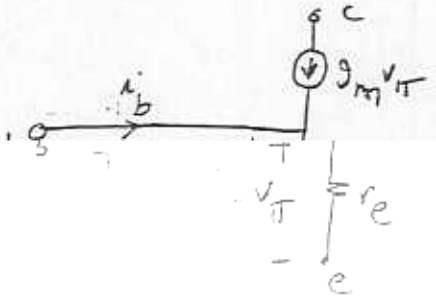
## Equivalent AC models of BJTs:




$$g_m = \frac{I_C}{V_T}, \quad r_\pi = \frac{\beta}{g_m}$$




$$r_\pi = \frac{\beta}{g_m}$$




$$r_e = \frac{V_T}{I_E}, \quad g_m = \frac{I_C}{V_T}$$

All these models are equivalent to each other and would give identical results.

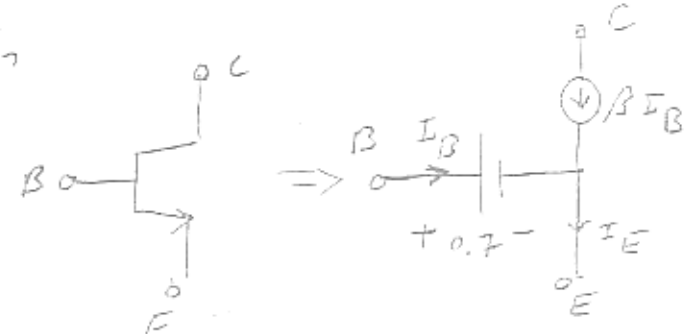
Meaning of very large $\beta$.

IF $\beta$ is large with BJT in active $\Rightarrow$

$I_C = \beta I_B$

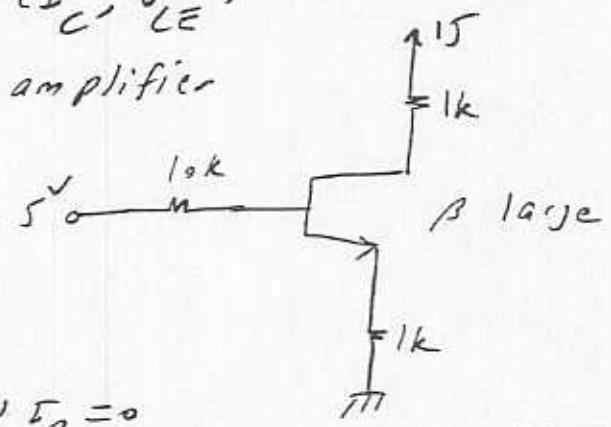
$I_E = (\beta+1) I_B \cong \beta I_B \Rightarrow$

$I_C \cong I_E$



When it is said that $\beta$ is large, its value is not given. For the Ac parameters $r_\pi$, you need $\beta$ value which is unknown. The way to work around this problem is to use the Third Ac model on page 1 which does not require the value of $\beta$. Find $I_E \cong I_C$ and then you can Find $r_e$ from $r_e = \frac{V_T}{I_E}$.

Ex. Find Dc operating Point $(I_C, V_{CE})$ and the Ac model For amplifier applications.




Assume active:

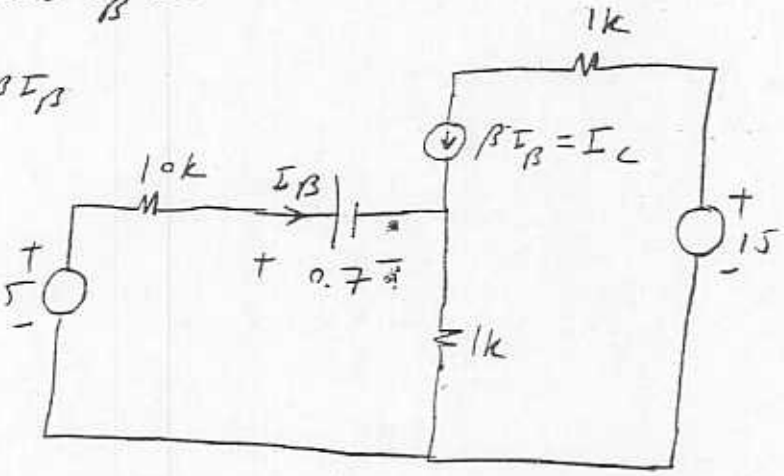
$KVL \Rightarrow -5 + 10k I_B + 0.7 + 1k(\beta+1) I_B = 0$

$\Rightarrow \beta >> 1 \Rightarrow 1k(\beta+1) I_B \cong 1k \beta I_B$

$\Rightarrow -5 + 10k I_B + 0.7 + 1k\beta I_B = 0$

$10k I_B + 1k\beta I_B = 1k I_B (\beta + 10)$

if $\beta$ very large ($\beta >> 10$) $\Rightarrow$

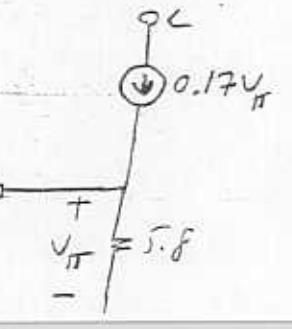



$-5 + 0.7 + 1k\beta I_B = 0 \Rightarrow I_C = \beta I_B = 4.3\,mA$

$KVL \Rightarrow -15 + 1k I_C + V_{CE} + 1k I_E = 0 \Rightarrow I_C \cong I_E \Rightarrow$

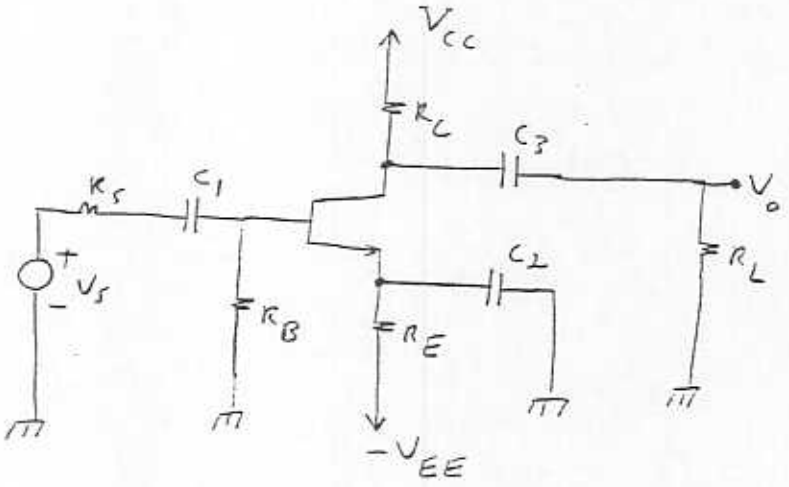
$V_{CE} = 15 - 4.3 - 4.3 = 6.4^V > 0.2 \checkmark$

$r_e = \frac{V_T}{I_E} = \frac{25m}{4.3m} = 5.8^\Omega \quad g_m = \frac{I_C}{V_T} \cong \frac{I_E}{V_T} = \frac{1}{r_e} = 0.17^U$

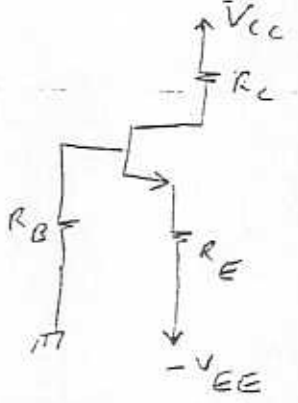


Common-emitter amplifier:

General configuration:

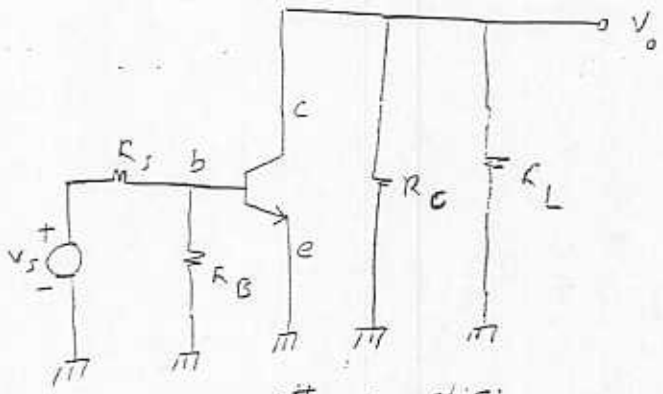



DC circuit:




BJT must be in active state

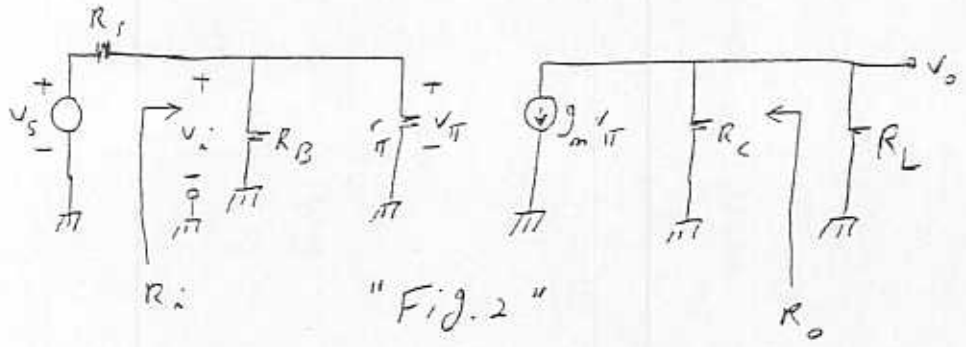
AC circuit:




Common-emitter amplifier.
Two ways to look at this and decide it is a CE amp.
1) emitter is grounded
2) $V_s$ is applied to base and $V_o$ is taken at the collector. emitter is shared between the input and output circuits.

"Fig. 1"

AC circuit:




"Fig. 2"

The Following equations hold For the AC circuit:

$$A_{V_o} = \frac{v_o}{v_i} = \frac{v_o}{v_\pi} = -g_m (R_C \| R_L) \qquad \text{amplifier gain}$$

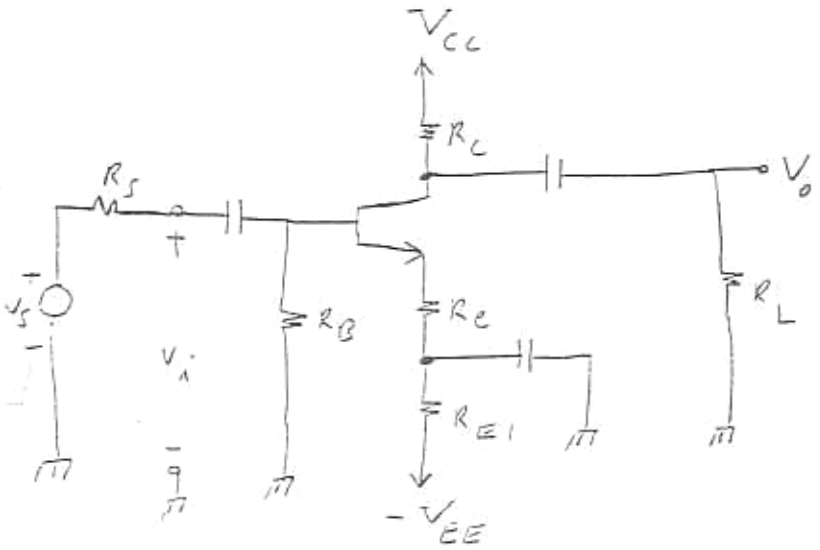
$$A_v = \frac{v_o}{v_s} = -\frac{(R_B \| r_\pi)}{(R_B \| r_\pi) + R_s} g_m (R_C \| R_L) \qquad \text{overall gain}$$

$R_i = R_B \| r_\pi$ input resistance of the amplifier

$R_o = R_C$ output resistance of the amplifier

Note that if the AC circuit For the BJT problem you are using looks like Fig. 1 or Fig. 2, then you can use the equations above to Find AC quantities without analysing the AC circuit

Ex. Common-emitter amplifier <u>with a resistance in the emitter:</u>



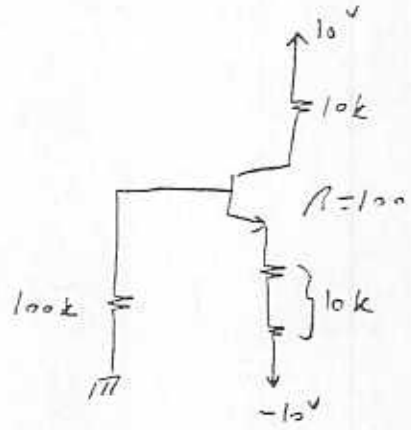

let $R_s = R_C = R_L = 10k$

$R_B = 100k$, $R_{E1} = 9830$

$R_e = 170$, $\beta = 100$

$V_{CC} = V_{EE} = 10^V$

DC Analysis:




This AC Problem was done in Handout #16.

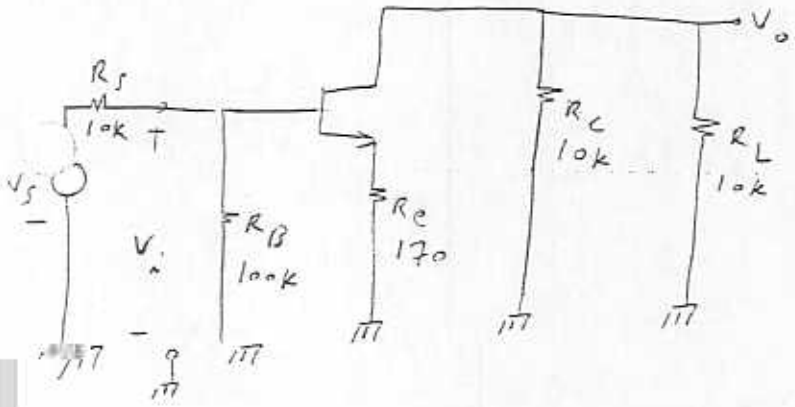
$I_C = 0.84\,mA$

$V_{CE} = 3.14\,V$

$g_m = 0.0336\,\mho$

$r_\pi = 3k$

AC Analysis:




For the AC small signal model of a BJT, we can use any of the two following models:

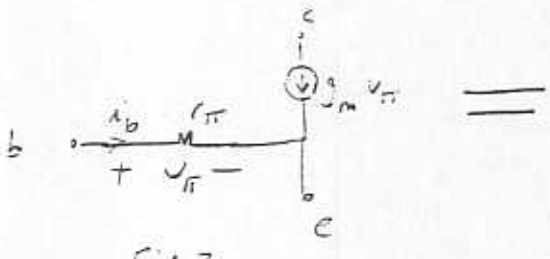



Fig. 3

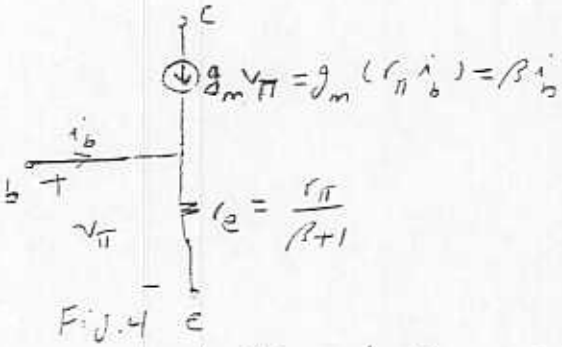



Fig. 4

These two models are completely equivalent and give identical results for AC quantities.

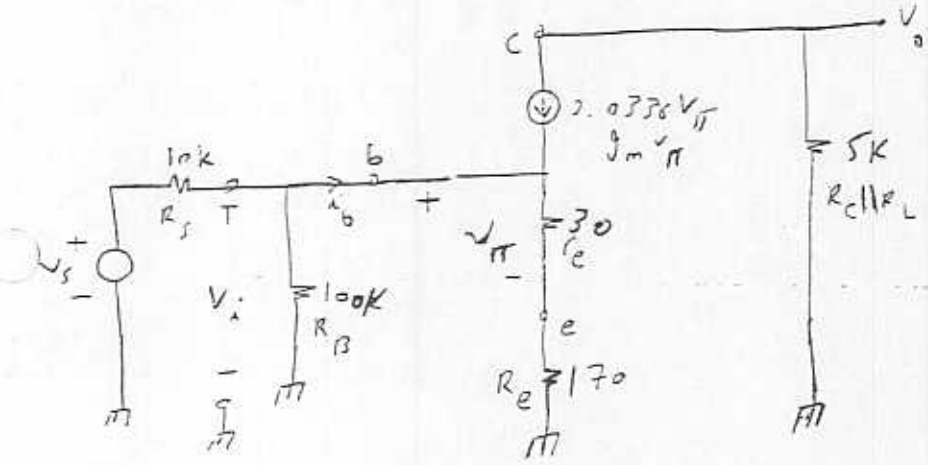
Note: Fig. 3 $\Rightarrow v_\pi = r_\pi i_b$, Fig. 4 $\Rightarrow v_\pi = r_e i_e = \frac{r_\pi}{\beta+1}(i_b + g_m v_\pi) = \frac{r_\pi}{\beta+1}(i_b + \beta i_b) = r_\pi i_b$

This means that both models give the same expression for $v_\pi = r_\pi i_b$ and $i_c = g_m v_\pi$. Therefore, they are identical.

For the common-emitter amplifier with a resistance in the emitter, it is more convenient to use the model in Fig. 4.

AC circuit:

$$r_e = \frac{r_\pi}{\beta+1} = \frac{3k}{101} \cong 30\,\Omega$$




① $\frac{V_o}{V_i}$:

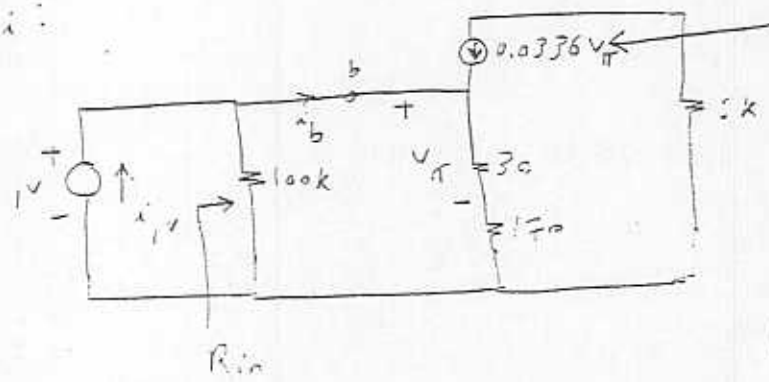
$V_o = -0.0336\, V_\pi\,(5k)$

KVL $\Rightarrow -V_i + V_\pi + 170\left(\frac{V_\pi}{30}\right) = 0 \Rightarrow V_\pi = 0.15\, V_i$

$V_o = -0.0336\,(5k)(0.15\, V_i) \Rightarrow V_o / V_i = -25.2$

$g_m V_\pi = \beta i_b$ (always)

② $R_i$:




$$R_{in} = \frac{1}{i_1 V}$$

KCL $\Rightarrow -i_1 V + \frac{1}{100k} + i_b = 0$ ①

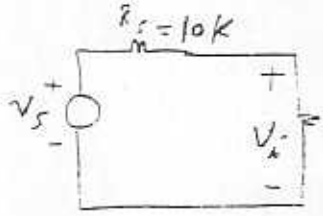
KVL $\Rightarrow -1 + 30\,(101\, i_b) + 170\,(101\, i_b) = 0$

$\Rightarrow i_b = \frac{1}{20200}$

① $\Rightarrow i_1 V = \frac{1}{100k} + \frac{1}{20.2k} \Rightarrow$

$R_{in} = \frac{1}{i_1 V} = 100k \,\|\, 20.2K = 16.8K$

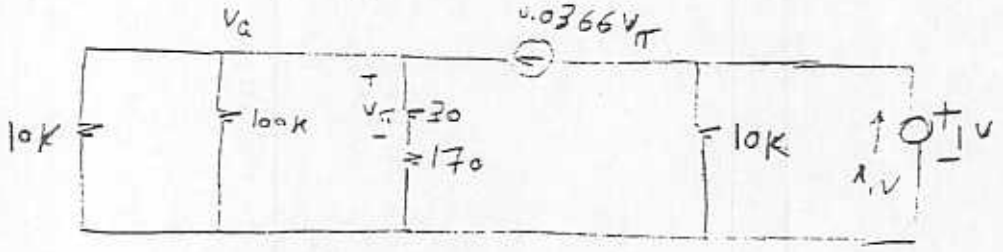
(3) $v_o/v_s$




$$v_i = \frac{16.8K}{10K+16.8K} v_s = 0.627 v_s$$

$$\frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = -25.2(0.627) = -15.8$$

(4) $R_{out}$ (excluding $R_L$).




$$v_a = v_\pi + \frac{v_\pi}{3\Omega}(17\Omega) = 6.67 v_\pi$$

$$KCL \Rightarrow \frac{6.67 v_\pi}{10K} + \frac{6.67 v_\pi}{100K} + \frac{v_\pi}{3\Omega} - 0.0366 v_\pi = 0 \Rightarrow v_\pi = 0$$

$$KCL \Rightarrow 0.0366 v_\pi + \frac{1}{10K} - \lambda_1 v = 0 \Rightarrow \lambda_1 v = \frac{1}{10K} \Rightarrow R_{out} = 10K$$

In terms of the variables shown in the AC circuit on P.3 or P.4, we have

$$\frac{v_o}{v_i} = -(R_C \| R_L)\frac{g_m}{1+\frac{R_e}{r_e}}$$

$$R_i = R_B \| [r_\pi (1+g_m R_e)]$$

$$\frac{v_o}{v_s} = -\frac{R_i}{R_i + R_s}(R_C \| R_L)\frac{g_m}{1+\frac{R_e}{r_e}}$$

$$R_{out} = R_C$$

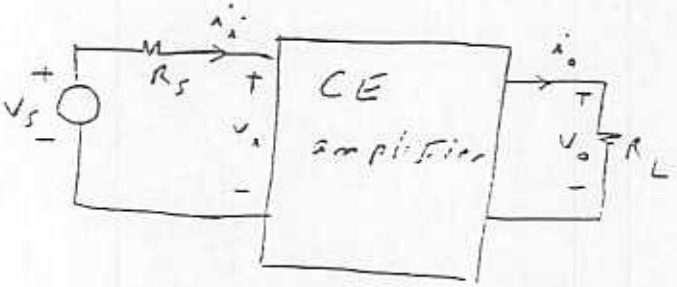
Again, if the AC circuit for a BJT looks like those shown on P.3 or P.4, we can use the equations above without analysing the the AC circuit.

Common-emitter amplifier in a nutshell:

A) No emitter resistor in the AC circuit:

1) $R_{in} = R_B \| r_\pi \cong r_\pi$ moderate input resistance (a few hundred to a few kilo ohm).

2) High voltage and current gain.




$$\frac{v_o}{v_i} = -g_m (R_C \| R_L)$$

$v_o/v_i$, $\frac{v_o}{v_s}$ and $\frac{i_o}{i_i}$ are all high

3) $R_{out} \cong R_C$ = collector resistor — high output resistance because $R_C$ is usually a few kΩ.

B) With emitter resistor in the AC circuit:

1) $R_{in} = R_B \| [r_\pi (1 + g_m R_e)]$

For $R_B$ chosen large, $R_{in}$ for the common-emitter (CE) amplifier with emitter resistance is much larger than the CE amplifier with no emitter resistor. Is this good or bad!

2) Moderately high voltage and current gains but not as high as those obtain with no emitter resistance

$$\frac{v_o}{v_i} = -(R_C \| R_L) \frac{g_m}{1 + \frac{R_e}{r_e}}$$

The gain $\frac{V_o}{V_i}$ with $R_e$ existing in the AC circuit is smaller than its counterpart in A by a factor of $1 + \frac{R_e}{r_e}$.

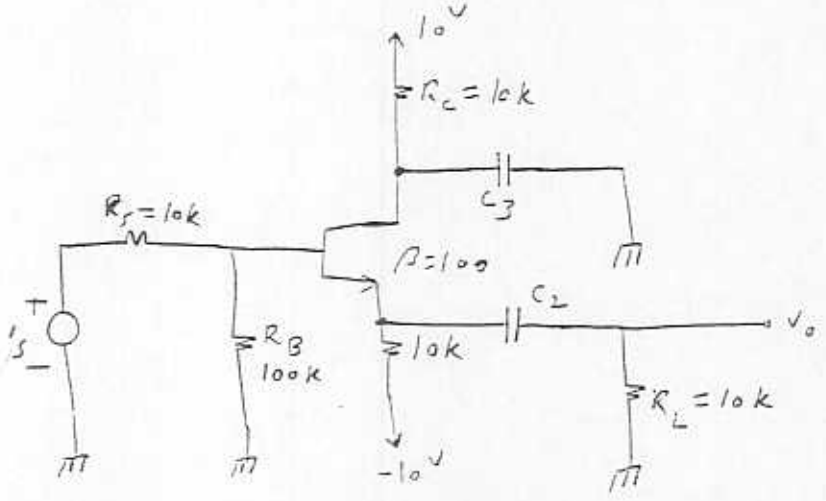
For the examples done before, this factor is $1 + \frac{170}{30} = 6.67$

The advantage of having emitter resistance in the AC circuit is that all gains (voltage and current) become less dependent on the BJT parameter $\beta$. This is good because $\beta$ varies a lot from one BJT to another.

c) $R_{out} = R_C$ same value with or without $R_e$

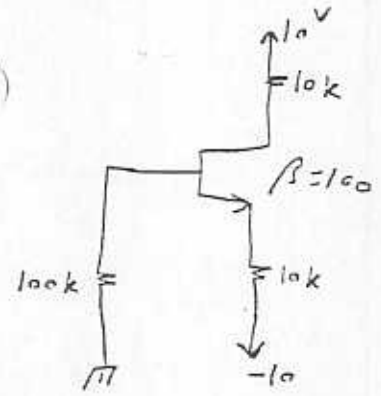
Note: $R_e$ is called a feedback resistor. If it is introduced in the AC circuit, it increases the input resistance and reduces all gains. Overall, $R_e$ is usually included in CE amplifiers because higher values of $R_{in}$ and gains not dependent on $\beta$ are desirable

Ex. Common-collector amplifier (emitter Follower):




Find $\frac{V_o}{V_S}$, $R_{in}$ after $V_S$ and $R_S$ and $R_{out}$ excluding the load $R_L$.

## (A) DC Analysis:




This is the same D.C problem as other examples.

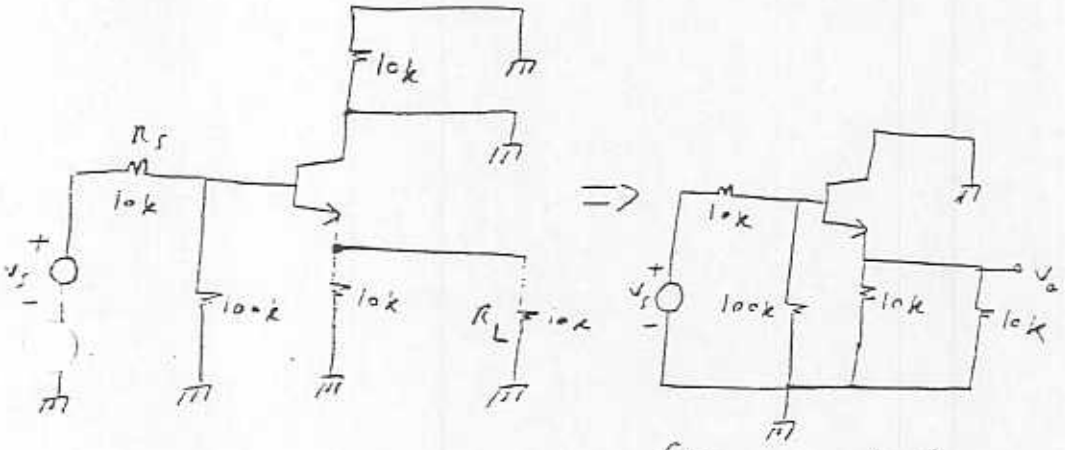
$I_C = 0.84\,mA$

$V_{CE} = 3.14\,V$

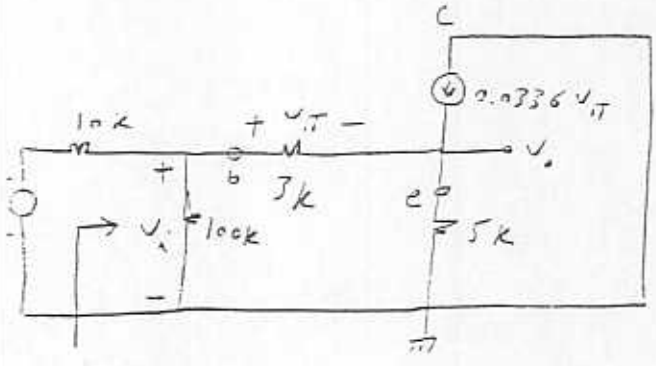
$g_m = 0.0336\,\mho$

$r_\pi = 3k$

## (B) AC Analysis:




Common-collector amplifier because $V_s$ is applied to base and output is taken at emitter. Collector is grounded.




(1) $V_o/V_i$:

$$V_o = 5k\left(0.0366\,V_\pi + \frac{V_\pi}{3k}\right) = 184.67\,V_\pi$$

$$KVL \Rightarrow -V_i + V_\pi + 5k\left(0.0366\,V_\pi + \frac{V_\pi}{3k}\right) \Rightarrow$$

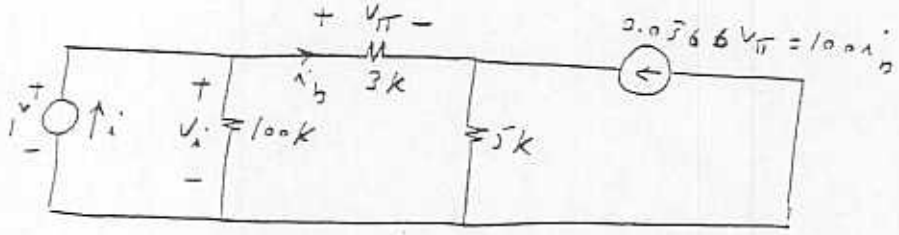
$$V_i = 185.67\,V_\pi$$

$$V_o = 184.67\left(V_i/185.67\right) = 0.9946$$

$$V_o/V_i = 0.9946 < 1$$

? what is this circuit good for? This circuit provides no voltage gain.

② $R_i$:




ⓐ

$KCL \Rightarrow -i + \frac{1}{100k} + i_b = 0$

$KVL \Rightarrow -1 + 3k\,i_b + 5k\,(101\,i_b) = 0$ ⓑ $\Rightarrow i_b = \frac{1}{508k}$

ⓐ $\Rightarrow i = \frac{1}{100k} + \frac{1}{508k} \Rightarrow R_{in} = \frac{1}{i} = 100k \,//\, 508k = 83.55k$

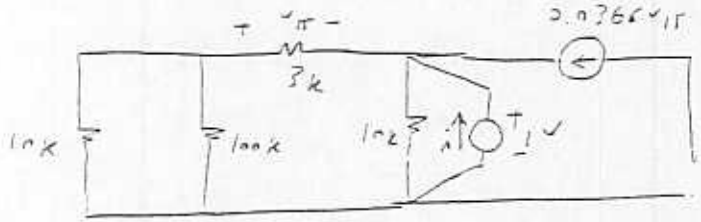
$R_{in}$ is definitely high. Is this good or bad?

③ $V_o/V_s$:

$$\frac{V_o}{V_s} = \frac{V_o}{V_i}\,\frac{V_i}{V_s} = 0.9946\,\frac{83.55k}{100k + 83.55k} = 0.89 < 1 \;?$$

$\frac{V_o}{V_s}$ has the same problem as $\frac{V_o}{V_i}$. It is smaller than 1. This circuit provides no voltage gain.

④ $R_{out}$:




$$V_\pi = \frac{3k}{100k \,//\, 100k + 3k}(-1) = -0.248$$

$KCL \Rightarrow -\frac{V_\pi}{3k} + \frac{1}{100k} - i - 0.0366\,V_\pi = 0 \Rightarrow i = 0.00926 \Rightarrow R_{out} = 108\,\Omega$

$R_{out}$ is very small. Is this good or bad?

This circuit is called an emitter follower because the emitter ($V_o$) follows the input ($V_i$ or $V_s$). Note that $V_o \cong V_i$ or $V_s$.

General equations For a CC amplifier:

$$\frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e}$$

$$\frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \quad \frac{R_E \| R_L}{R_E \| R_L + r_e}$$

$$R_i = R_B \left\| \left[ (\beta+1)(r_e + R_E \| R_L) \right] \right.$$

$$R_{out} = R_E \left\| \quad \frac{r_\pi + R_s \| R_B}{\beta+1} \right.$$

IF the Ac circuit For a BJT problem looks like those shown on P 3, these equations can be used without analysing the AC circuit.

---

sections covered: 4.11

ENGR. 364

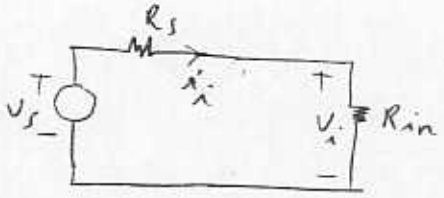
Handout # 18

supplement

CC amplifier problem continued:

(1) Find current gain = $A_i = \frac{i_o}{i_i}$

$i_o = v_o/R_L$, $i_i = \frac{v_s}{R_s + R_{in}}$




$$\frac{i_o}{i_i} = \frac{v_o/R_L}{v_s/(R_s+R_{in})} = \frac{R_s+R_{in}}{R_L} \quad \frac{v_o}{v_s} = \frac{10k + 83.55k}{10k}(0.89) = 8.32 > 1$$

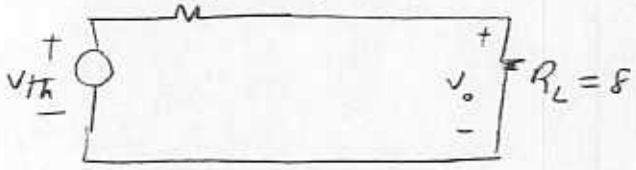
There is current gain

(2) Find power gain = $\frac{\text{AC Power across load}}{\text{AC Power To the amplifier}} = \frac{v_o^2/R_L}{v_i^2/R_{in}} = \left(\frac{v_o}{v_i}\right)^2 \frac{R_i}{R_L}$

$= (0.9948)^2 \left(\frac{83.55k}{10k}\right) = 8.26$

There is power gain. IF your load is a speaker ($R_L = 8$), your Power gain can become very high.

(3) Note that this circuit is very appropriate For driving a speaker because it has small $R_{out}$.




Note that $R_{out} = 10\Omega$ is still very large to drive a speaker. We can design the CC amplifier to give $R_{out} \cong 1\Omega$ which is more appropriate.

(4) Find maximum value of $v_s = A\sin\omega t$ allowed For SSA to hold.

$v_o = 184.67 v_\pi \Rightarrow 0.89 v_s = 184.67 v_\pi \Rightarrow v_\pi = \frac{0.89 v_s}{184.67} \leq 10mV \Rightarrow$

$v_s \leq 2.074 \Rightarrow v_s|_{max} = A = 2.047^V$

(5) What is the maximum value of $v_s$ allowed to avoid the amplifier from going to saturation.

we need $v_{CE} = V_{CE} + v_{ce} \geq 0.2 \Rightarrow$

Ac circuit $\Rightarrow v_{ce} + v_o = 0 \Rightarrow v_{ce} = -v_o = -0.89 v_s$

$\Rightarrow 3.14 - 0.89 v_s \geq 0.2 \Rightarrow v_s \leq 3.3^{V} \Rightarrow v_s|_{max} = A = 3.3^{V}$

⑥ what is the maximum value of $v_s$ allowed to avoid the amplifier from going to cut off.

we need $i_C = I_C + i_c \geq 0 \Rightarrow 0.84m + 0.0336 v_{IT} \geq 0 \Rightarrow$

$0.84m + 0.0336 \left( \frac{0.89 v_s}{184.67} \right) \geq 0 \Rightarrow v_s \geq -5.187^{V} \Rightarrow$

$v_s|_{max} = A \leq 5.187^{V}$

Note that

$v_s \leq 2.074$ For 55A

$v_s \leq 3.3$ to avoid saturation

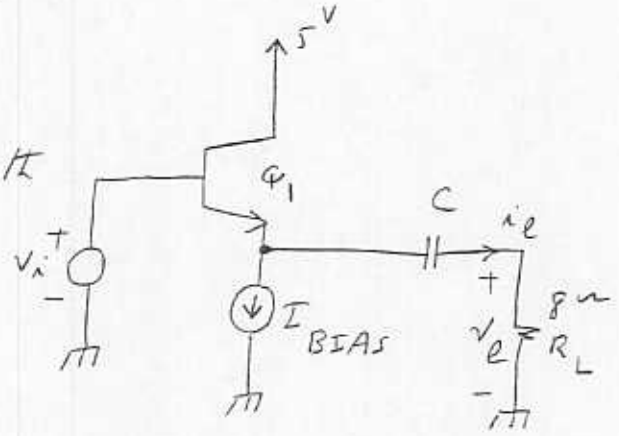
$v_s \leq 5.187$ to avoid cut-off

keep $v_s \leq 2.074$ To satisfy all three.

# ENGR. 164
# Lab #7 Handout

## 1) Ideal class A power amplifier:

Goal: Deliver 0.25W AC power to the 8Ω load.




Note that even though there are both DC and AC supplies in the network, $R_L$ only has an AC voltage and current as obvious from $v_e$ and $i_e$ notation. This is because the capacitor is open in the DC circuit not allowing any DC current or voltage for $R_L$.

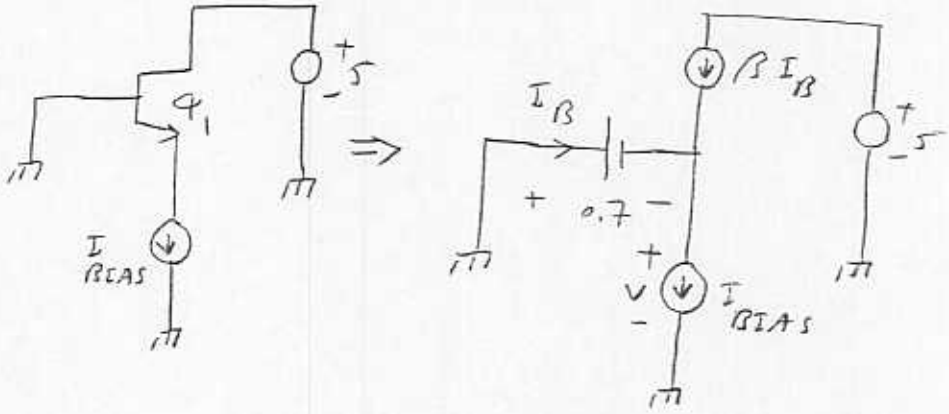
DC Problem: Assume active

KVL $\Rightarrow +0.7+V=0 \Rightarrow V=-0.7$

KVL $\Rightarrow -5+V_{CE}+V=0 \Rightarrow$

$V_{CE}=5.7>0.2$ ✓

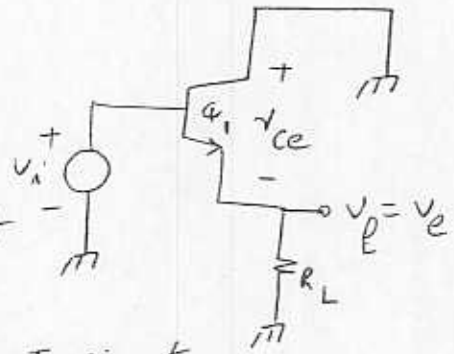
$I_C \cong I_E = I_{BIAS}$

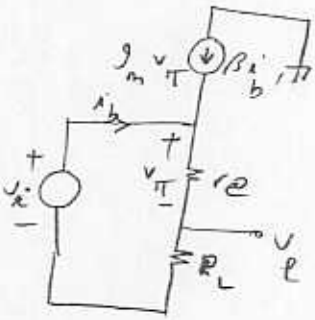


AC problem:

Let $v_i = A\sin\omega t \Rightarrow$

load voltage and current are also sinusoidal.




$$v_e = \frac{R_L}{R_L + r_e} v_i = \frac{R_L}{R_L + r_e} A\sin\omega t = V_{em}\sin\omega t$$

$$v_e = R_L i_e \Rightarrow i_e = \frac{V_{em}}{R_L}\sin\omega t = I_{em}\sin\omega t$$

Again, note that $R_L$ has only AC voltage and current.

Power dissipated by $P_L = \frac{V_{em}^2}{2R_L}$ (From ENGR. 320) $\Rightarrow$

$$V_{em} = \sqrt{2R_L P_L}, \quad I_{em} = \frac{V_{em}}{R_L} = \sqrt{2\frac{P_L}{R_L}}$$

Need $P_L = \frac{1}{4}\,W \Rightarrow V_{em} = \sqrt{2(8)(\frac{1}{4})} = 2\,V$ = required amplitude of load voltage for $P_L = 1/4\,W$

$$I_{em} = \sqrt{2\frac{P_L}{R_L}} = \sqrt{2\frac{(1/4)}{8}} = 0.25A = \text{required amplitude of load current for } P_L = 1/4\,W$$

AC circuit $\Rightarrow v_{ce} + v_e = 0 \Rightarrow v_{ce} = -v_e$, $i_c = \frac{\beta}{\beta+1} i_e \cong i_e = i_L$

To avoid saturation $\Rightarrow v_{CE} = V_{CE} + v_{ce} = 5.7 - v_e \geq 0.2 \Rightarrow v_e \leq 5.5$

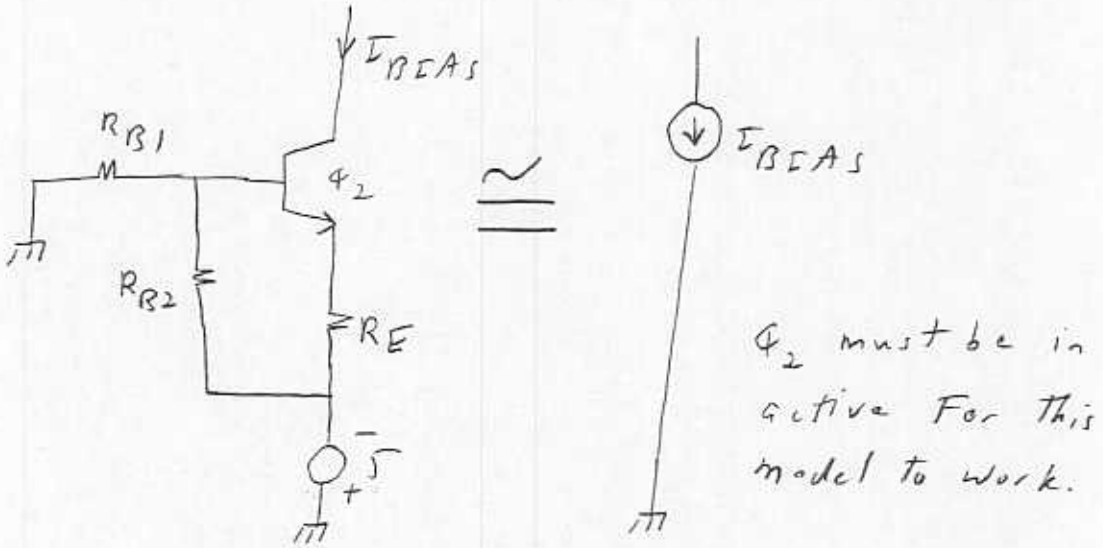
since $v_e|_{max} = V_{em} = 2\,V$, $v_e \leq 5.5$ is satisfied.

To avoid cutoff, $i_C = I_C + i_c = I_{BIAS} + i_L \geq 0 \Rightarrow i_L \geq -I_{BIAS}$

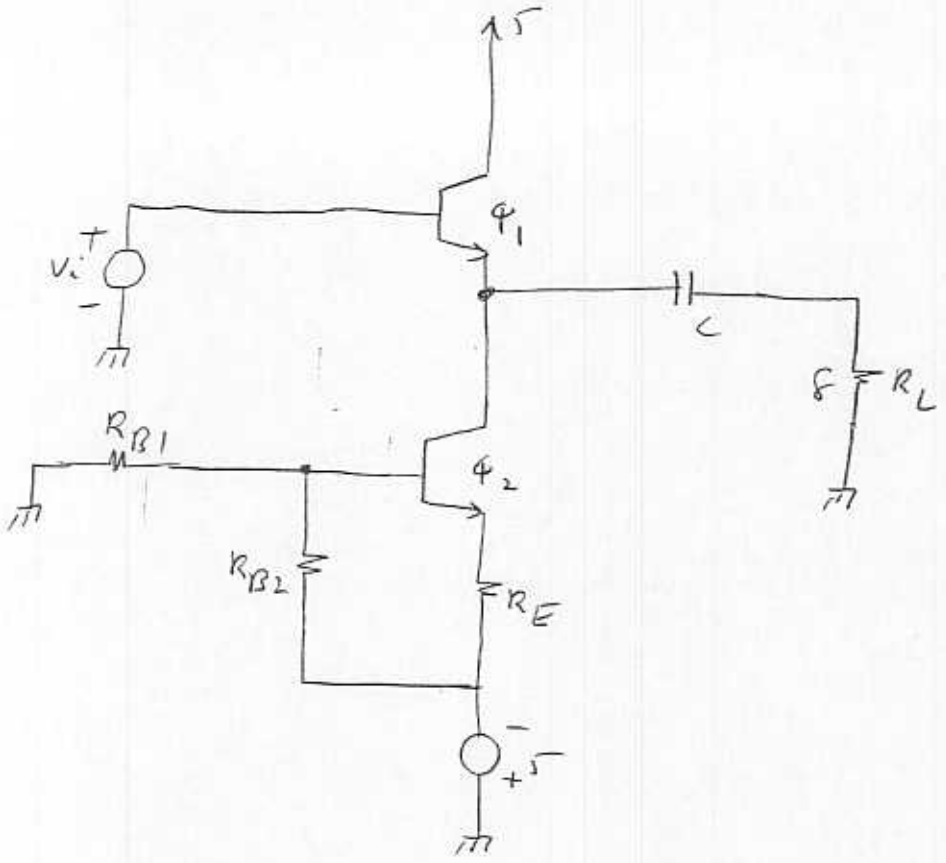
$-I_{em} \leq i_L \leq +I_{em} \Rightarrow i_L\big|_{min} = -I_{em} = -0.25 \geq -I_{BIAS} \Rightarrow I_{BIAS} \geq 0.25 \Rightarrow$ choose $I_{BIAS} = 0.3$

Choose $I_{BIAS} = 0.3$ to avoid cutoff.

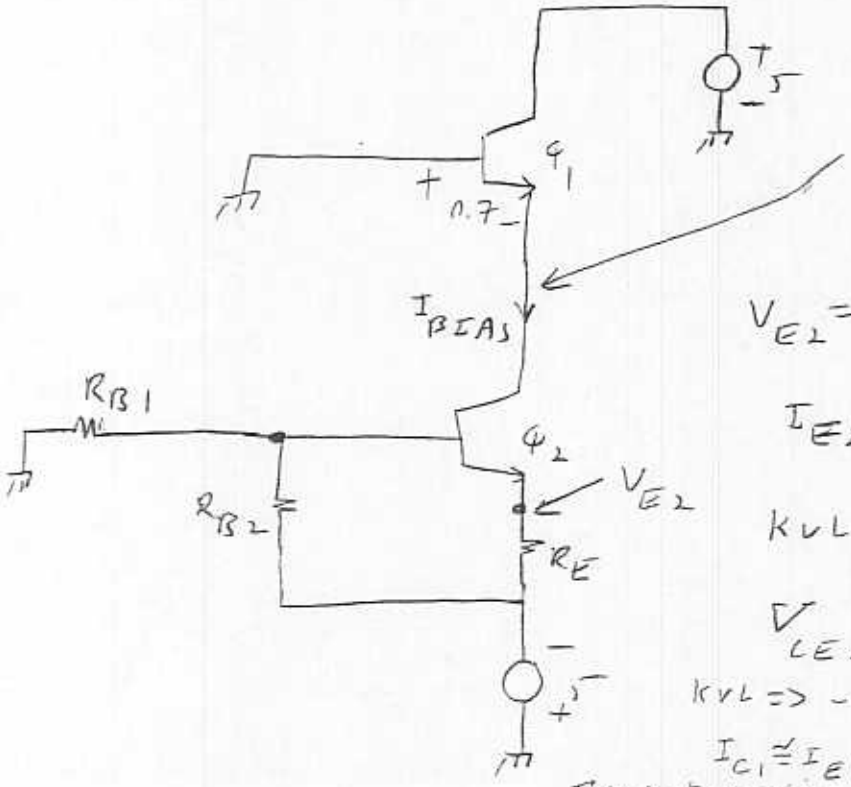
At this point, we have designed the amplifier such that for $P_L = \frac{1}{4}W$ requiring $V_{em} = 2^V$ and $I_{em} = 0.25^A$, the BJT always stays in active avoiding saturation and cut off. This required $I_{BIAS} = 0.3^A$. The problem with this ideal power amplifier is that a current source ($I_{BIAS}$) does not exist in real-life. One way to model $I_{BIAS}$ in real life is shown below.




A real-life power amplifier is often shown below replacing $I_{BIAS}$ in the ideal picture with $Q_2$ Transistor shown above.




DC problem:




Note that in the DC problem, collector current of $Q_2$ must be $I_{BIAS}$ just like the ideal case.

$$V_{E2} = R_E I_{E2} - 5 \Rightarrow$$

$$I_{E2} \cong I_{BIAS} = \frac{V_{E2}+5}{R_E}$$

$$KVL \Rightarrow 0.7 + V_{CE2} + V_{E2} = 0 \Rightarrow$$

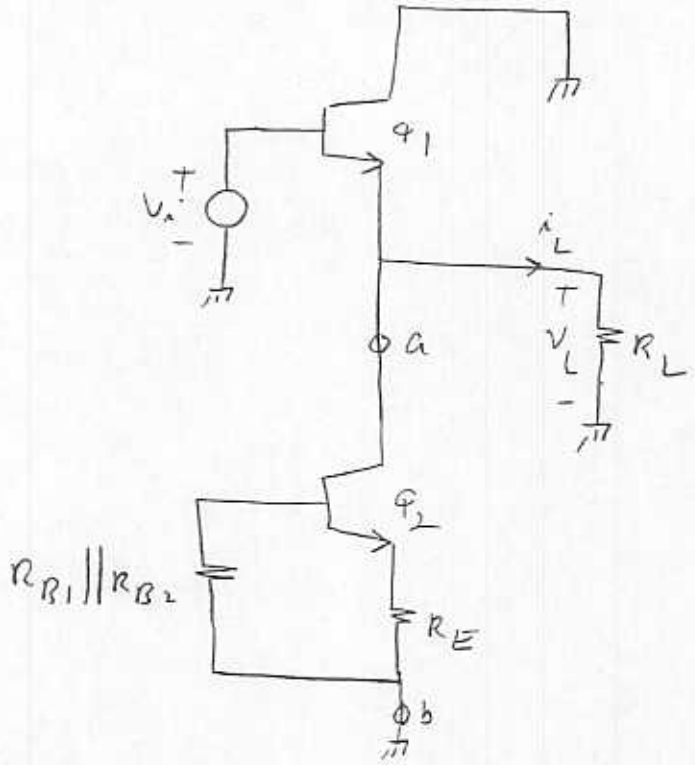
$$V_{CE2} = -0.7 - V_{E2}$$

$$KVL \Rightarrow -5 + V_{CE1} - 0.7 = 0 \Rightarrow V_{CE1} = 5.7 \text{ V}$$

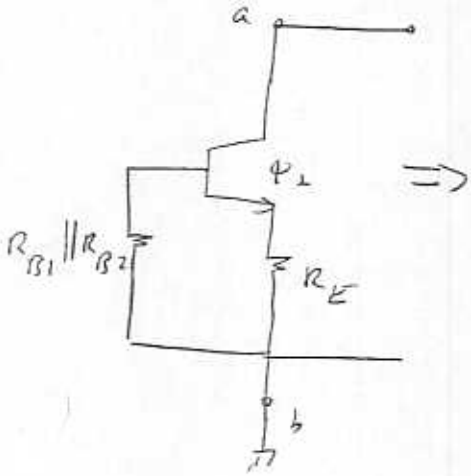
$$I_{C1} \cong I_{E1} = I_{C2} \cong I_{E2} = I_{BIAS} = 0.3 \text{ A}$$

This last equation is true since $Q_1$ & $Q_2$ are in active

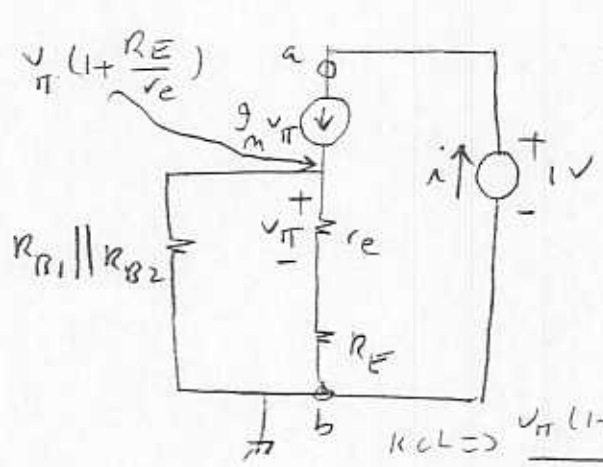
Ac Problem:




Between the collector of $Q_2$ and ground (terminals a and b), we can replace the circuit by a simple $R_{eq}$. Let's find $R_{eq}$ between a and b and replace everything between a and b by $R_{eq}$.




$\Rightarrow$

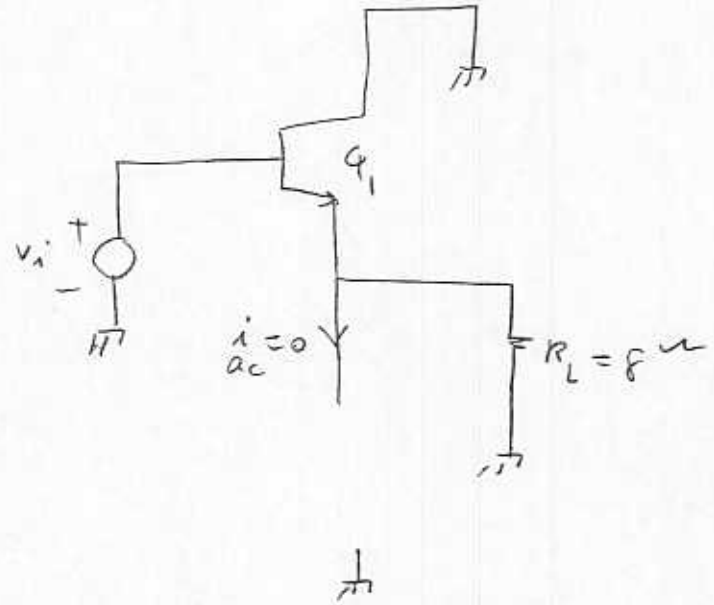



KCL $\Rightarrow \dfrac{V_\pi (1 + \frac{R_E}{r_e})}{R_{B1} \| R_{B2}} + \dfrac{V_\pi}{r_e} - g_m V_\pi = 0 \Rightarrow$

$V_\pi = 0 \Rightarrow i = g_m v_\pi = 0 \Rightarrow$

$R_{eq} = 1/i = \infty$ !

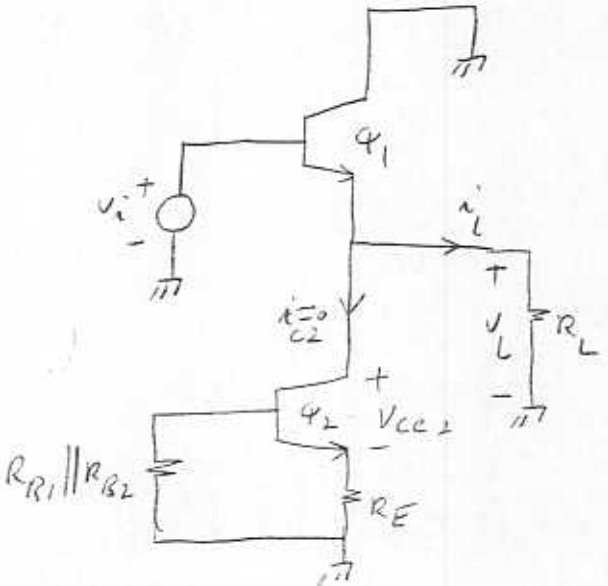
The equivalent circuit now becomes




This is exactly the same AC circuit as for the ideal case.

This really proves that $Q_2$ circuit was acting like a DC current source of value $I_{BIAS}$ which became open in the AC problem.

Now, let's consider one more time, the AC circuit that has $Q_2$ in it.




$i_{C2} = i_{E2} = 0$ because $R_{EG} = \infty$.

KVL $\Rightarrow -V_L + V_{CE2} + R_E(i_{E2}) = 0 \Rightarrow$

$V_{CE2} = V_L$

For $Q_2$ To stay in active, $V_{CE2} \geq 0.2 \Rightarrow$

$V_{CE2} + V_{CE2} \geq 0.2 \Rightarrow -0.7 - V_{E2} + V_L \geq 0.2 \Rightarrow$

$V_{E2} \leq V_L - 0.9$

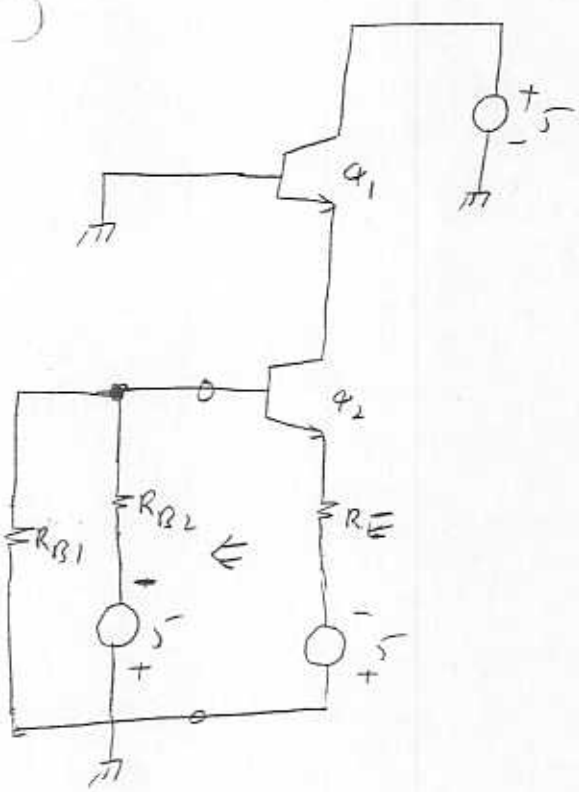
$-V_{em} \le V_L \le V_{em} \Rightarrow V_{E2} \le -V_{em} - 0.9 = -2.9^V$ choose $V_{E2} = -3^V$

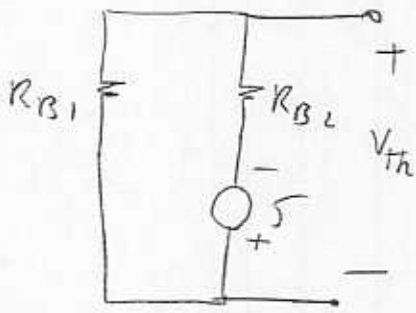
$I_{BIAS} = \frac{V_{E2}+5}{R_E}$ From DC analysis on p.4 $\Rightarrow$

$0.3 = \frac{-3+5}{R_E} \Rightarrow R_E = 6.7^\Omega$ choose Three $22^\Omega$ resistors in parallel For $R_E$ giving

$R_E = 22 \| 22 \| 22 = 7.3^\Omega \cong 6.7^\Omega$

To complete the design of the real life amplifier, we need to Find $R_{B1}$ and $R_{B2}$. Let's look at the DC problem again.

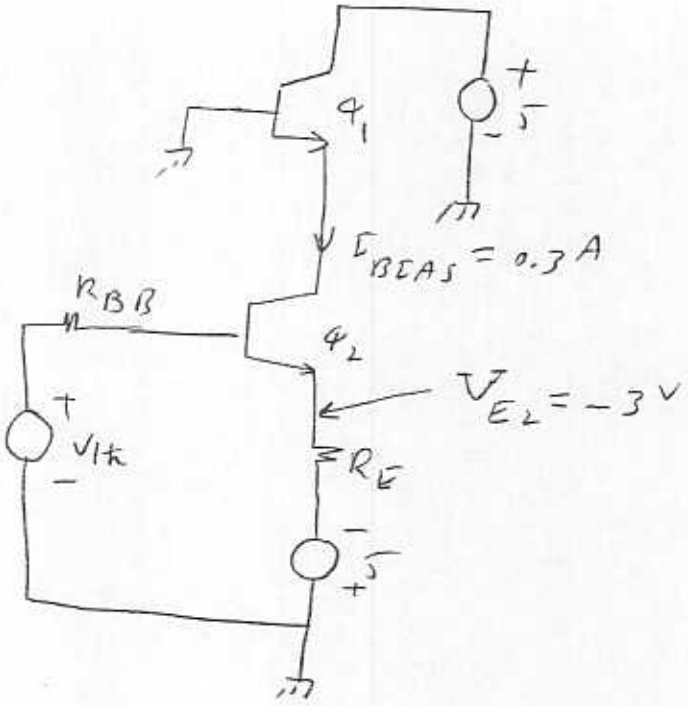



$V_{th} = -\frac{R_{B1}}{R_{B1}+R_{B2}} 5$

$R_{th} = R_{B1} \| R_{B2} = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}}$

Dc circuit becomes




KVL $\Rightarrow -V_{th} + R_{BB} I_{B2} + 0.7 + R_E (\beta+1) I_{B2} - 5 = 0$ eq. (1)

Choose $R_{BB} I_{B2} << R_E (\beta_2+1) I_{B2}$ to make $I_{E2}$ independent of $\beta_2$. Why?

IF $R_{BB} I_{B2} << R_E (\beta_2+1) I_{B2} \Rightarrow$

KVL becomes

$-V_{th} + 0.7 + R_E I_{E2} - 5 = 0 \Rightarrow$

$I_{E2} = \dfrac{V_{th} + 4.3}{R_E} \cong I_{BIAS}$ indep. of $\beta_2$.

This is good because we need $I_{BIAS} = 0.3$ independent of $\beta_2$ of $Q_2$.

$R_{BB} I_{B2} << R_E (1+\beta_2) I_{B2} \Rightarrow$ let $R_{BB} I_{B2} = 0.1 R_E (1+\beta_2) I_{B2}$

$\Rightarrow R_{BB} = 0.1 R_E (1+\beta_2)$. $\beta_1$ and $\beta_2$ are typically around 80. $\Rightarrow$

$R_{BB} = 0.1(7.3)(81) = 60\,\Omega$

eq. (1) $\Rightarrow + \dfrac{R_{B1}}{R_{B1}+R_{B2}} 5 + 60\left(\dfrac{0.3}{80}\right) + 0.7 + 7.3(0.3) - 5 = 0$

$$\frac{R_{B1}}{R_{B1}+R_{B2}} = 0.415$$

We also have

$$\frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = R_{BB} = 60 \Rightarrow R_{B2} = \frac{60}{0.415} = 144\ \Omega$$

$$\Rightarrow R_{B1} = 0.415R_{B1} + 0.415R_{B2} \Rightarrow R_{B2} = 203\ \Omega$$

Choose $R_{B1} = R_{B2} = 120\ \Omega$ This gives $R_{BB} = R_{B1} \| R_{B2} = 60\ \Omega$,

$$\frac{R_{B1}}{R_{B1}+R_{B2}} = 0.5 \cong 0.415$$

Design is now complete.

Let's compute power dissipation by different elements.

Dc Power dissipation:

$P_{Q1} = I_{C1}V_{CE1} = 0.3(5.7) = 1.71$ watts see Dc circuit on P. 4

Note that KVL $\Rightarrow -5 + V_{CE1} - 0.7 = 0 \Rightarrow V_{CE1} = 5.7\ V$

$P_{Q2} = I_{C2}V_{CE2}$, $I_{C2} = I_{E1} \cong I_{C1} = 0.3\ A$ (see P.4)

KVL $\Rightarrow -5 + V_{CE1} + V_{CE2} + V_{E2} = 0 \Rightarrow V_{CE2} = 5 - 5.7 + 3 = 2.3\ V$ (see P.4)

$P_{Q2} = 0.3(2.3) = 0.69\ W$

$P_{R_{BB}} = R_{BB}(I_B)^2 = 60\left(\frac{0.3}{80}\right)^2 = 0.84\ mW$

$P_{R_E} = R_E (I_{E2})^2 = 7.3(0.3)^2 = 0.657\ W$

$P(V_{th}) = V_{th} I_{B2} = 2.5(0.3/80) = 0.009\ W$ why is $V_{th}$ dissipating power.

Total DC Power dissipated $= P_{q_1} + P_{q_2} + P_{R_{BB}} + P_{R_E} + P_{V_{th}} = 1.71 + 0.69 + 0.00084 + 0.657 + 0.009 = 3.06\ W$

we could have also computed the total power dissipated as power supplied by the DC voltages which must be equal to total power dissipated. Let's check this.

Total DC power supplied $= 5 I_{C1} + 5 I_{E2}$

$= 5(0.3) + 5(0.7) = 3\ W$ close enough!

Power calculations For DC+AC together!

$i_{C1} = I_{C1} + i_{c1} = 0.3 + i_L$ (see P.6 AC circuit)

$\Rightarrow i_{C1} = 0.3 + 0.25 \sin \omega t$

$v_{CE1} = V_{CE1} + v_{ce1} = 5.7 - V_L$ (see P.6 AC circuit)

$v_{CE1} = 5.7 - 2 \sin \omega t$

$P_{q_1}(t) = (5.7 - 2\sin \omega t)(0.3 + 0.25 \sin \omega t)$

$P_{q_1}(\text{average}) = 5.7(0.3) - \frac{1}{4} = 1.46\ W$

$i_{C2} = I_{C2} + i_{c2} = 0.3 + 0$ (remember $R_{eq} = \infty \Rightarrow$ No AC current through $q_2$)

$v_{CE2} = V_{CE2} + v_{ce2} = 2.3 + V_L$ (see AC circuit on P.6) $\Rightarrow$

$v_{CE2} = 2.3 + 2\sin\omega t$

$P_{Q_2}(t) = (2.3 + 2\sin\omega t)\, 0.3$

$P_{Q_2}(\text{average}) = 2.3(0.3) = 0.69$ watts

All other average powers $P_{R_E}$, $P_{R_{BB}}$, $P_{V_{th}}$ are the same as before. Only $P_{Q_1}$ went down by $0.25$ W. ⇒

$P_{\text{average}}(\text{total dissipated}) = 3\text{ W} - 0.25$ (less power in $Q_1$)

$+ 0.25 = 3$ W

↑ Power dissipated in $R_L$

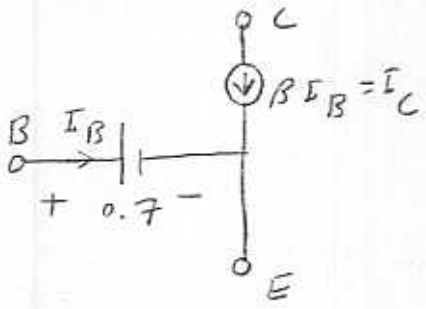
$$\text{Efficiency} = \frac{P_{R_L}}{P(\text{total})} = \frac{0.25}{3} = 8.3\%$$ very low!

# BJT exam review

## (1) BJT DC Problems (DC supplies):

BJT can be in saturation, active or cutoFF.

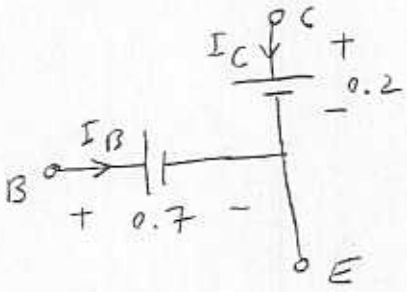
Active:



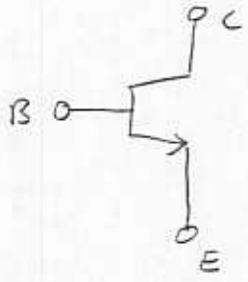

verify $V_{CE} \geq 0.2$

or $V_{CB} \geq 0$

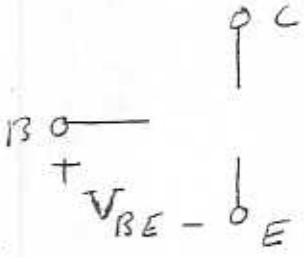
Saturation:




verify $I_C < \beta I_B$



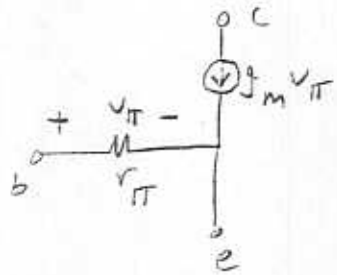

Cutoff:

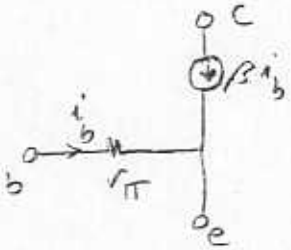


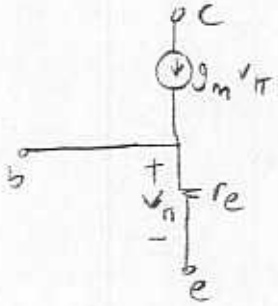

verify $V_{BE} < 0.7$

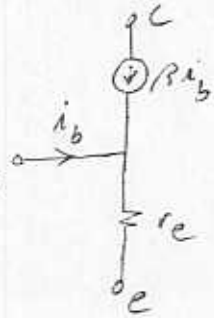
## (2) BJT AC Problems: (BJT DC circuit must have BJT in active state).

BJT is used as an amplifier.



All the AC models shown are correct and must give identical results. We have

$$r_e = \frac{r_\pi}{\beta+1}, \quad v_\pi = r_\pi i_b, \quad v_\pi = r_e(\beta+1) i_b = r_e i_e, \quad g_m v_\pi = \beta i_b$$

For the exam you must be able to find the following AC quantities:

A) Find $\frac{v_o}{v_i}$, $\frac{v_o}{v_s}$, $R_{in}$, $R_{out}$ for amplifiers.

B) Find all $v_s$ for BJT to satisfy SSA ($v_{be} \leq 10mV$)

C) Find all $v_s$ for BJT to avoid saturation ($v_{CE} = V_{CE} + v_{ce} \geq 0.2$).

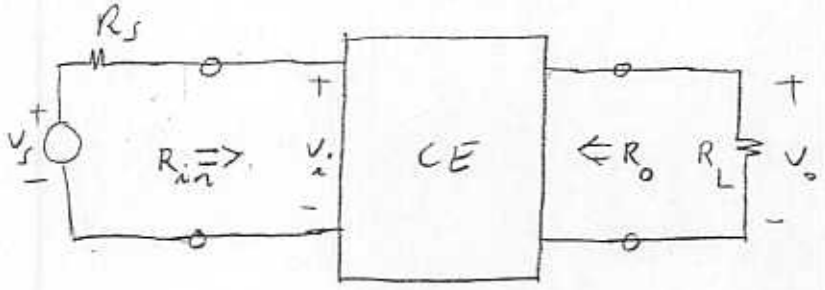
D) Find all $v_s$ for BJT to avoid cut off ($i_C = I_C + i_c \geq 0$).

IF your AC problem looks like a CE, CE with emitter resistance $R_e$ or CC amplifier, use the standard equations given in handouts to find AC quantities.

IF the AC problem does not look like a CE, CE with emitter resistance $R_e$ or CC amplifier, you have to solve the AC problem by writing KCL or KVL.

Some important properties of amplifiers:

A) CE amplifier:

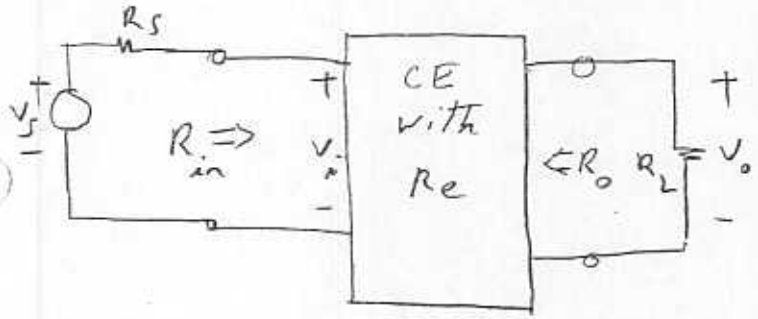



$R_i = R_B \| r_\pi$ a few hundred ohms to a few K$\Omega$.

$R_o = R_C$ a few k$\Omega$

$\frac{V_o}{V_i}$, $\frac{V_o}{V_S}$ both are big, Ten to hundred.

B) CE amplifier with emitter resistance $R_e$.

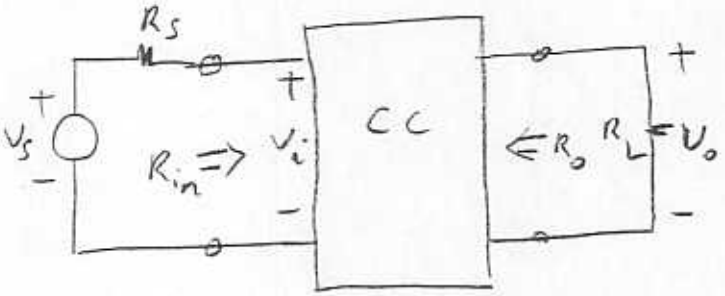



$R_i = R_B \| [r_\pi (1 + g_m R_e)]$ a few k$\Omega$

$R_o = R_C$ a few k$\Omega$

$\frac{V_o}{V_i}$, $\frac{V_o}{V_S}$ are both big but smaller than a CE amplifier. Ten to Fifty.

C) CC amplifier




$R_i$ large, 50 to 200 k$\Omega$.

$R_o$ small 10 to 120 $\Omega$.

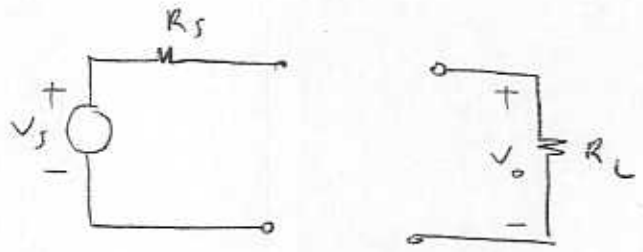
$\frac{V_o}{V_i}$, $\frac{V_o}{V_S} \simeq 1$ (unity gain)

Note: CE amplifier with $R_e$ is preferred to simple CE amplifier because its $\frac{V_o}{V_i}$ and $\frac{V_o}{V_S}$ are not sensitive to variations in $\beta$ value of BJT.

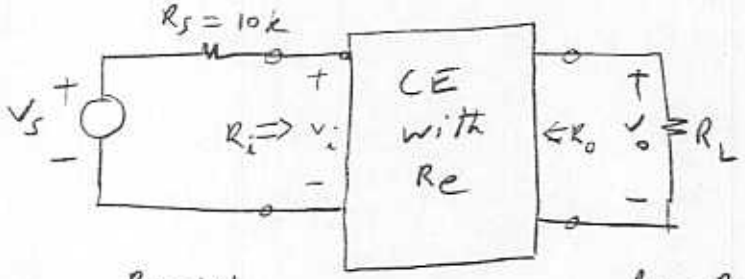
Let's study some applications of BJT amplifiers.

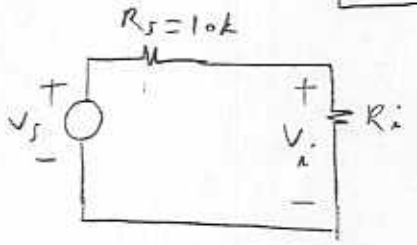
Suppose you have an AC power supply and a load $R_L$.

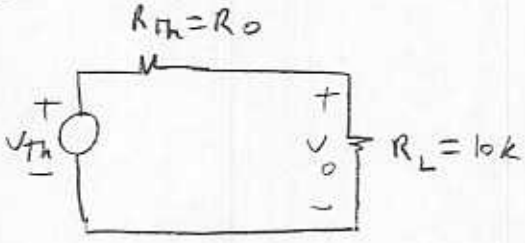
Let's see how they should be connected to each other depending on the values of $R_S$, $R_L$ and problem specifications.




① $R_S = 10k$, $R_L = 10k$, need voltage gain $\frac{V_o}{V_S} >> 1$.



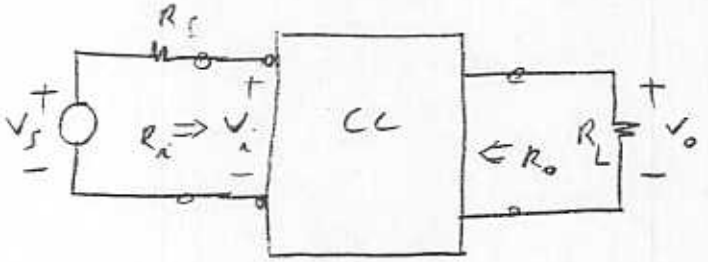




$R_i$ is a few kΩ $\Rightarrow$ $V_i$ is a good portion of $V_S$.

$R_L$ and $R_o$ (a few kΩ) are comparable $\Rightarrow$ $V_o$ is a good portion of $V_{Th}$. Amplification is provided by CE with $R_e$ configuration ($\frac{V_o}{V_S} >> 1$). $\frac{V_o}{V_S} >> 1$ can be either understood by just saying that we are using a

CE with $R_e$ amplifier which gives $\frac{V_o}{V_s} >> 1$. The other way to come to the same conclusion, which we have never done) is to find $V_{th}$ for the amplifier. This is the output open-circuit voltage excluding $R_L$. You will get something like $V_{th} = -100 V_s$. If $R_o$ and $R_L$ are then let's say equal to each other, we will get $V_o = \frac{V_{th}}{2} = -50 V_s \Rightarrow \frac{V_o}{V_s} = -50$. In class, we have never found $V_{th}$ but either way to convice yourself $\frac{V_o}{V_s} >> 1$ is ok.

(2) $R_s = 20k$, $R_L = 10\Omega$, no need for voltage gain ($\frac{V_o}{V_s}$ can be 1).

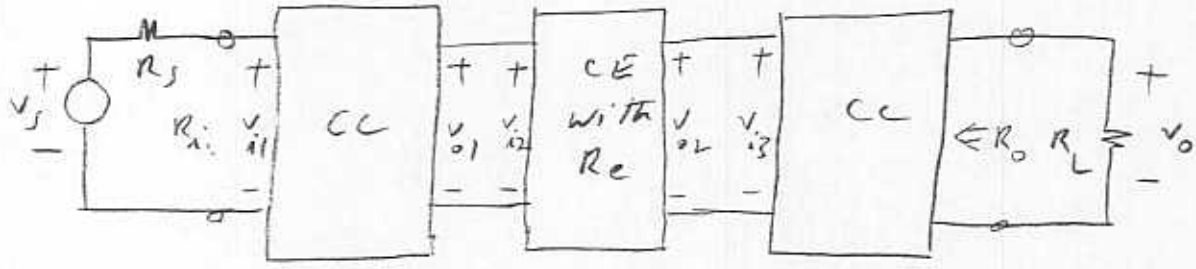



$R_i$ bigger or comparable to $R_s$ ✓

$R_o$ comparable to $R_L$ ✓

$\frac{V_o}{V_s} \cong 1$ ✓

(3) $R_s = 50k$, $R_L = 10\Omega$, need voltage gain $\frac{V_o}{V_s} >> 1$




$R_i$ comparable to $R_s$ ✓ $R_o$ comparable to $R_L$ ✓

$V_{o1}/V_s \cong 1$, $V_{o2}/V_{i2} >> 1$, $V_o/V_{i3} \cong 1 \Rightarrow \frac{V_o}{V_s} = \frac{V_{o1}}{V_s} \cdot \frac{V_{o2}}{V_{o1}} \cdot \frac{V_o}{V_{o2}} = \frac{V_{o1}}{V_s} \cdot \frac{V_{o2}}{V_{i2}} \cdot \frac{V_o}{V_{i3}} >> 1$ ✓

ENGR.364
Handout #20

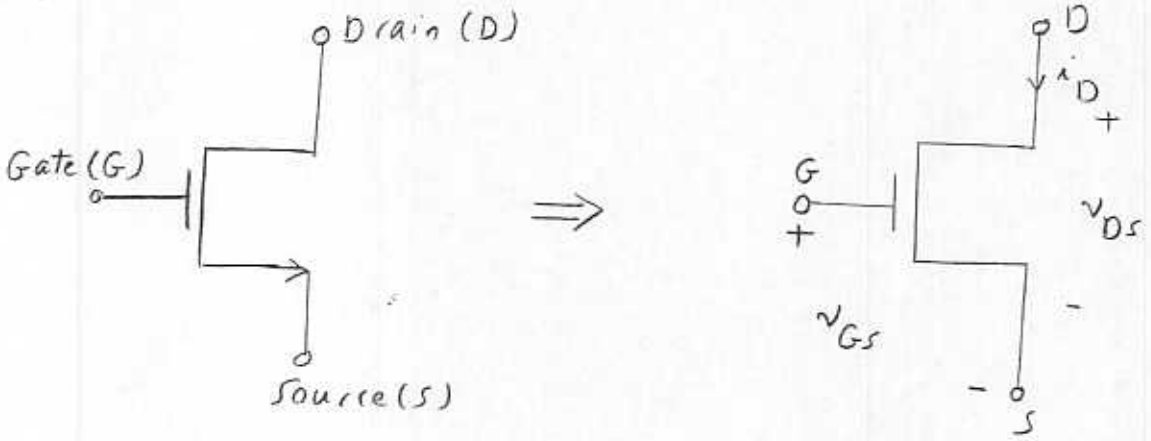
Metal oxide semiconductor Field Effect Transistors (MOSFET):

There are two types of MOSFETs.

- MOSFET
  - enhancement-type MOSFET
    - n type (NMOS)
    - P type (PMOS)
  - depletion-type MOSFET
    - n type (NMOS)
    - P type (PMOS)

We will study NMOS type MOSFETs for both enhancement and depletion types.

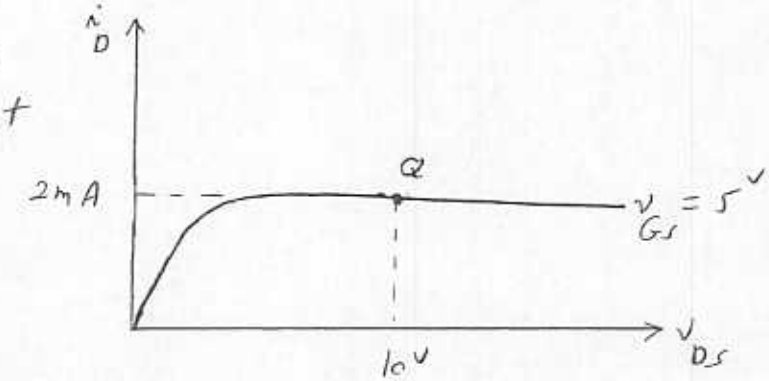
Enhancement type MOSFET (n channel):



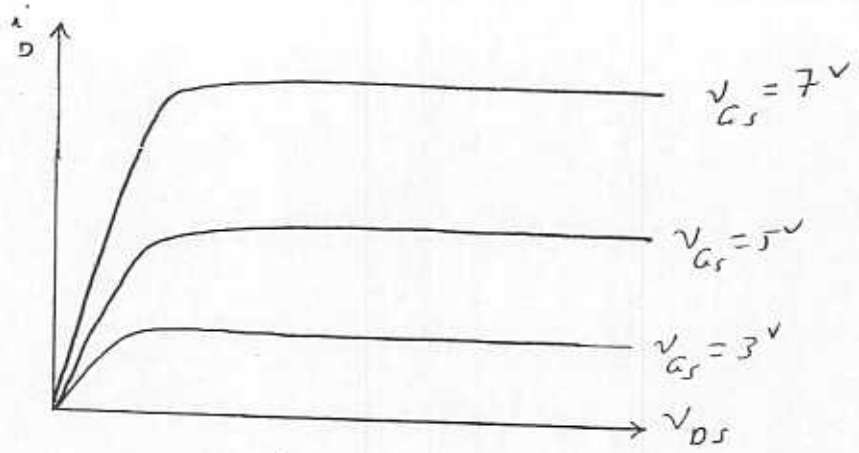

Note that all voltages and currents have the notation for total (DC+AC) signals. For a given value of $v_{GS}$, the $i_D - v_{DS}$ curve is shown below.

Point Q represents a typical operating point of the MOSFET.

$$\begin{cases} v_{GS} = 5^{V} \\ i_D = 2mA \\ v_{DS} = 10^{V} \end{cases}$$



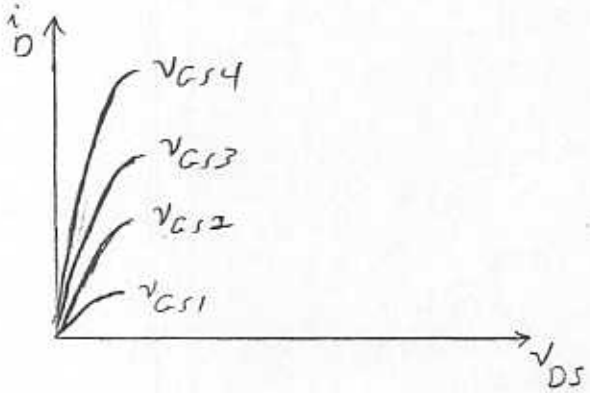
Since $v_{GS}$ can take on different values, we get one curve for each $v_{GS}$ value.




The value of $v_{GS}$ determines what curve we are on. The values of $i_D$ and $v_{DS}$ would then determine one point on that curve. This point is the operating point of the MOSFET.

A MOSFET can have three regions of operations:

① The linear region is called triode region.




In triode, we have

$$i_D = k\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right]. \quad (1)$$

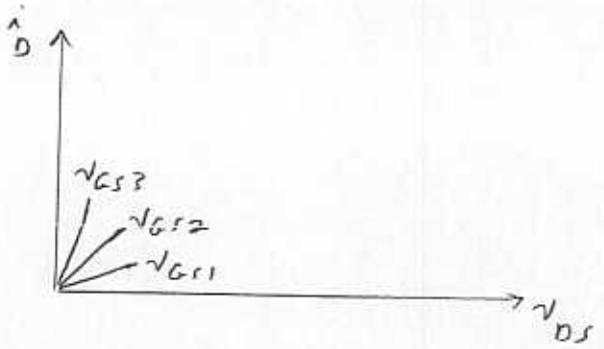
k is a constant specified by the manufacturer. $V_t$ is called the threshold voltage. It is also specified by the manufacturer. Both these parameters depend on the fabrication process.

This equation means that for a given value of $v_{GS}$, the relationship between $i_D$ and $v_{DS}$ is quadratic and goes according to eq. 1.

If $v_{DS}$ is sufficiently small, we can neglect the $v_{DS}^2$ term.

$$i_D = k\left[2(v_{GS} - V_t)v_{DS}\right].$$

The relationship between $i_D$ and $v_{DS}$ is now perfectly linear.



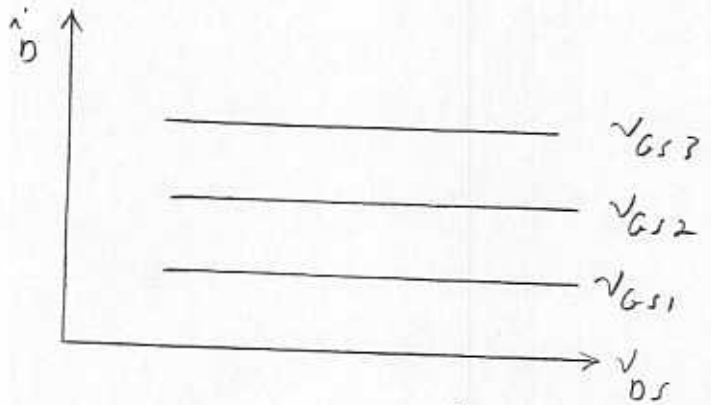

This relationship represents the operation of MOSFET as a linear resistor of value $r_{DS} = \frac{v_{DS}}{i_{DS}} = \left[2K(v_{GS} - V_t)\right]^{-1}$. The value of the resistor is controlled by $v_{GS}$ because it depends on $v_{GS}$. When $v_{DS}$ is sufficiently small in triode region, the MOSFET can be used as a voltage-controlled resistor.

In triode region, the following inequalities must hold.

$$v_{GS} > V_t$$

$$v_{DS} \leq v_{GS} - V_t$$

(2) The flat portions of the curves are called saturation region




In saturation, we have $i_D = K(v_{GS} - V_t)^2$ independent of $v_{DS}$. This is also clear from the graph that shows $i_D$ for a given $v_{GS}$ does not change with $v_{DS}$.

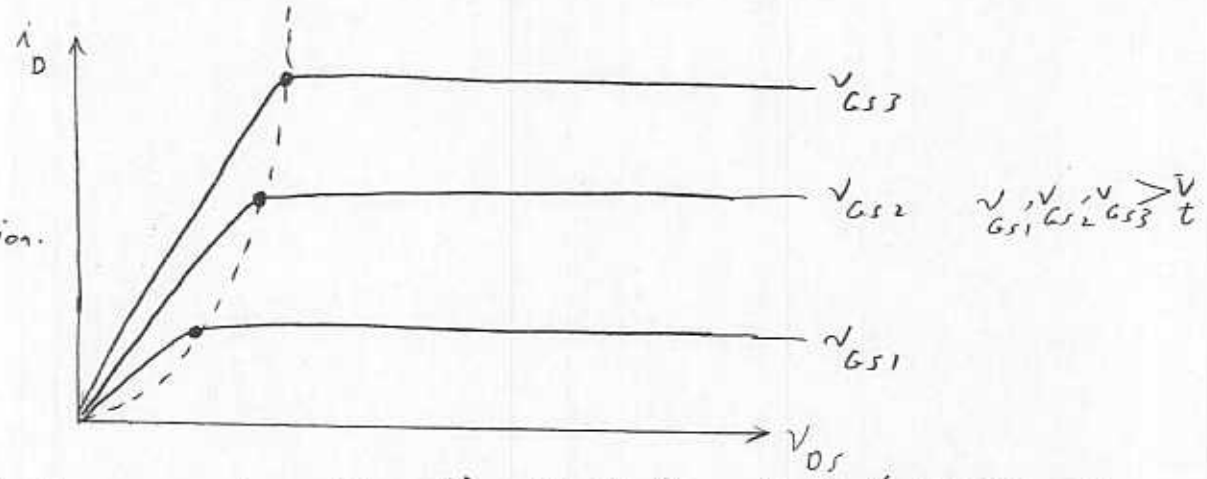
In saturation, the following inequalities must hold

$$v_{GS} > V_t$$

$$v_{DS} \geq v_{GS} - V_t$$

Note that both triode and saturation have $v_{GS} > V_t$. $v_{DS} = v_{GS} - V_t$ defines the boundary between triode and saturation.

- represents the boundary between triode and saturation.




Along the dashed curve, $v_{DS} = v_{GS} - V_t$. Along the dashed curve, we can either use

$$i_D = k\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right]$$

or

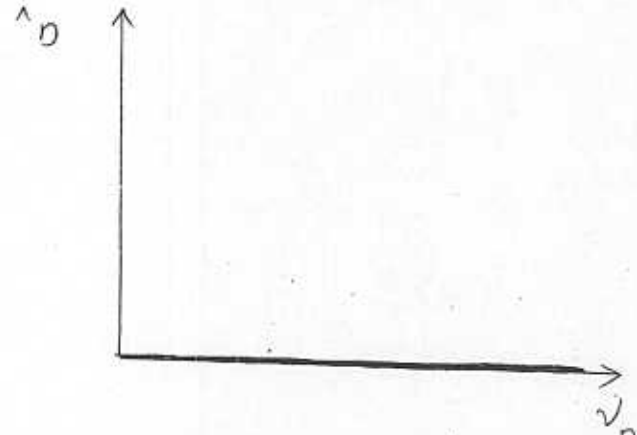
$$i_D = k(v_{GS} - V_t)^2$$

to express the $i_D \perp v_{DS}$ curve of the MOSFET. This is because we are at the boundary of the two regions and both equations are correct. Using $i_D = k(v_{GS} - V_t)^2$ and $v_{DS} = v_{GS} - V_t$ together gives

$$\underline{\underline{i_D = k v_{DS}^2}} \text{ along the dashed curve.}$$

Using $i_D = k\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right]$ together with $v_{DS} = v_{GS} - V_t$ also gives the same equation. This implies that $i_D \perp v_{DS}$ curve along the boundary between saturation and triode goes as $i_D = k v_{DS}^2$.

(3) Cut OFF:

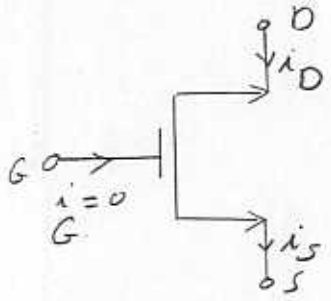



$i_D = 0$

$v_{GS} \leq V_t$

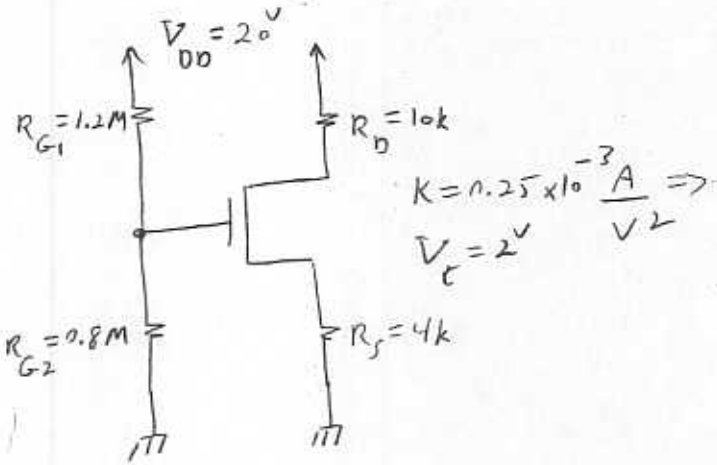
Anytime, the voltage $v_{GS}$ is below or equal to threshold voltage, the MOSFET will be in cut off.

Note that For a MOSFET, $i_G = 0$ regardless of the state of operation of the MOSFET



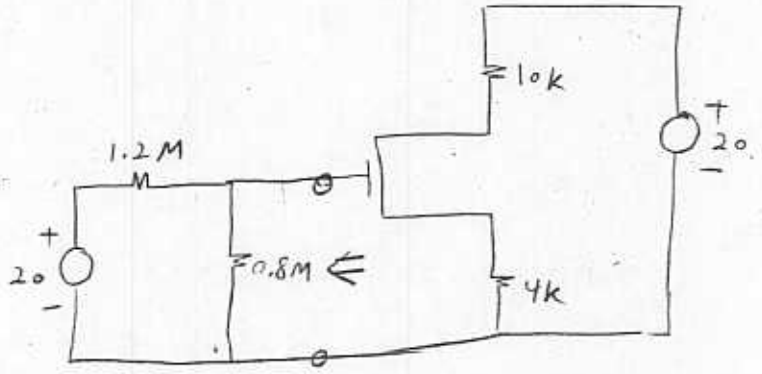

$i_D = i_S$

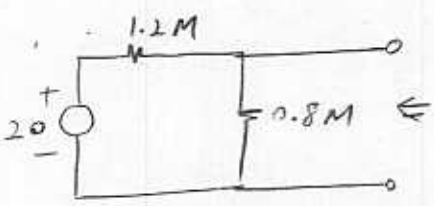
EX.1. Find $I_D$ and $V_{DS}$




$K = 0.25 \times 10^{-3} \frac{A}{V^2} \Rightarrow$

$V_t = 2^V$



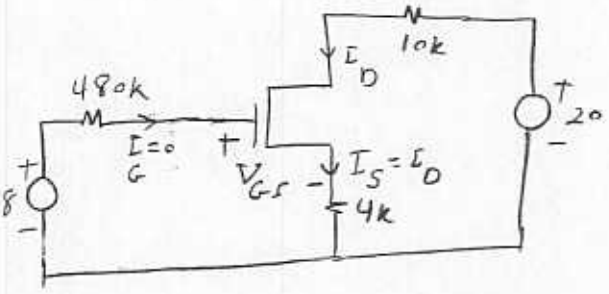




$V_{Th} = \frac{0.8M}{0.8M + 1.2M} 120) = 8^V$

$R_{Th} = 0.8M \parallel 1.2M = 480k$

Assume saturation (pinch off):

$$\text{KVL} \Rightarrow \begin{cases} \text{①}\ -8 + 480k\,(0) + V_{GS} + 4k\,I_D = 0 \quad (i_G = 0) \\ \text{②}\ I_D = k(V_{GS} - V_t)^2 = 0.25\times10^{-3}(V_{GS}-2)^2 \end{cases}$$




Note that because all power supplies are DC, we use $V_{GS}$, $I_D$, $V_{DS}$, ...

$$\text{①} \Rightarrow I_D = \frac{8 - V_{GS}}{4k}$$

$$\text{②} \Rightarrow \frac{8 - V_{GS}}{4k} = 0.25\times10^{-3}(V_{GS}-2)^2 \Rightarrow V_{GS}^2 - 3V_{GS} - 4 = 0 \Rightarrow V_{GS} = 4, -1$$

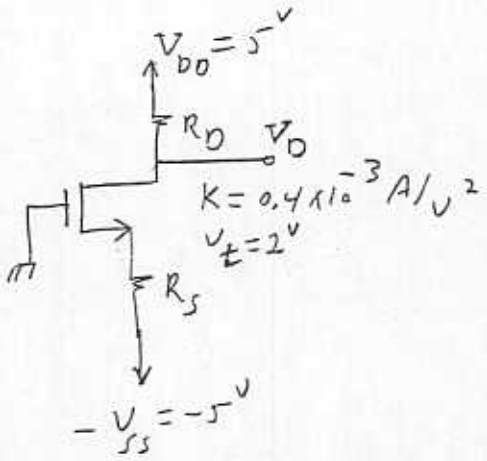
We need $V_{GS} > V_t = 2$ in pinch off $\Rightarrow$ choose $V_{GS} = 4 > V_t = 2$ ✓

$$\text{①} \Rightarrow I_D = \frac{8 - V_{GS}}{4k} = 1mA$$

$$\text{KVL} \Rightarrow -20 + 10k(1m) + V_{DS} + 4k(1m) = 0 \Rightarrow V_{DS} = 6\ V$$

$$V_{DS} = 6 > V_{GS} - V_t = 4 - 2 = 2 \quad ✓$$

Ex. Find $R_D$ and $R_S$ to get $I_D = 0.4mA$ and $V_D = 1^V$.




Assume pinch off $\Rightarrow$

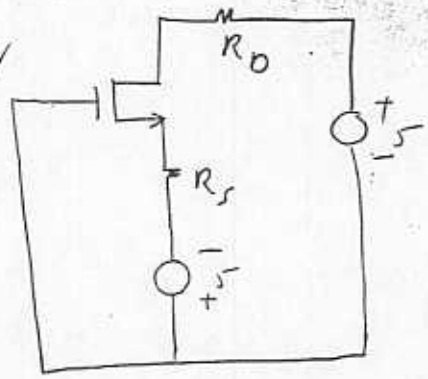
$I_D = K(V_{GS} - V_t)^2 \Rightarrow$

$0.4 \times 10^{-3} = 0.4 \times 10^{-3}(V_{GS} - 2)^2 \Rightarrow$

$(V_{GS} - 2)^2 = 1 \Rightarrow V_{GS} - 2 = \pm 1 \Rightarrow$

$V_{GS} = 3, 1$

we need $V_{GS} > V_t = 2 \Rightarrow$ choose $V_{GS} = 3^V$ ✓




KVL $\Rightarrow V_{GS} + R_S I_D - 5 = 0 \Rightarrow$

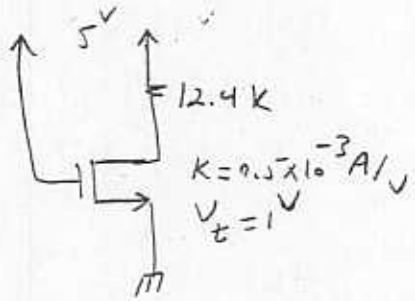
$3 + R_S(0.4 \times 10^{-3}) - 5 = 0 \Rightarrow R_S = 5k$

$V_D = 1 = -R_D(0.4 \times 10^{-3}) + 5 \Rightarrow$

$R_D = 10k$

KVL $\Rightarrow -5 + 10k(0.4m) + V_{DS} + 5k(0.4m) - 5 = 0 \Rightarrow V_{DS} = 4 \geq V_{GS} - V_t = 1^V$ ✓

Ex. Find $I_D$ and $V_{DS}$.




Assume pinch off $\Rightarrow$

$I_D = K(V_{GS} - V_t)^2 = 0.5 \times 10^{-3}(5-1)^2 = 8mA$

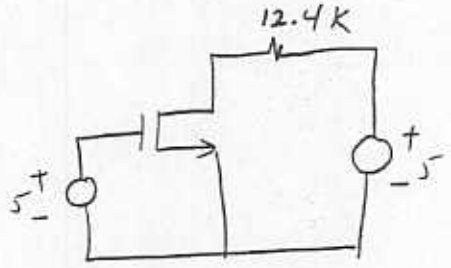
$V_{GS} = 5^V > V_t = 1$ ✓

KVL $\Rightarrow -5 + 12.4K(8m) + V_{DS} = 0 \Rightarrow$

$V_{DS} = -94.2 \geq V_{GS} - V_t = 5 - 1 = 4$ ✗

Assume triode $\Rightarrow$

$V_{GS} = 5 > V_t$ ✓



$I_D = k[2(V_{GS} - V_t)V_{DS} - V_{DS}^2] \Rightarrow I_D = 0.5\times10^{-3}(8V_{DS} - V_{DS}^2)$

KVL $\Rightarrow -5 + 12.4K I_D + V_{DS} = 0$

$$\begin{cases} I_D = 0.5\times10^{-3}(8V_{DS} - V_{DS}^2) \\ I_D = \dfrac{5 - V_{DS}}{12.4k} \end{cases} \Rightarrow 0.5\times10^{-3}(8V_{DS} - V_{DS}^2) = \frac{5 - V_{DS}}{12.4k} \Rightarrow$$

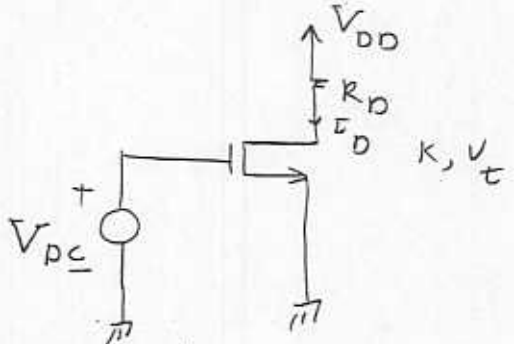
$V_{DS} = 0.1, 8.06$

In triode, we need $V_{DS} \leq V_{GS} - V_t = 5 - 1 = 4 \Rightarrow$ choose $V_{DS} = 0.1$ V

$I_D = \dfrac{5 - 0.1}{12.4K} = 0.395\,mA$

MOSFETs as amplifiers:

For an enhancement MOSFET to act as an amplifier of an AC supply, we first need to bias the MOSFET in the saturation or pinch-off (flat portion of the i-v curve) using DC supplies.




we now have

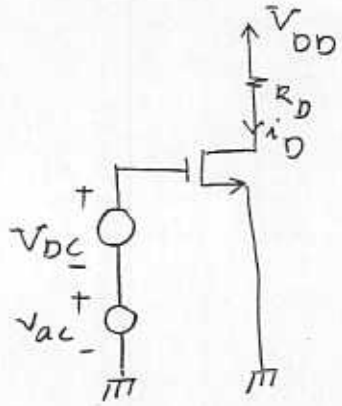
KVL $\Rightarrow V_{GS} = V_{DC}$

$I_D = k(V_{GS} - V_t)^2$

Verify $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$.

KVL $\Rightarrow -V_{DD} + R_D I_D + V_{DS} = 0 \Rightarrow V_{DS} = V_{DD} - R_D I_D \geq V_{GS} - V_t$

Next, we superimpose an AC supply $v_{ac}$ on top of $V_{DC}$ which is the AC supply that is to be amplified. This AC supply must be small enough in magnitude not to drive the MOSFET out of pinch off.




We, now, have

$$\text{KVL} \Rightarrow v_{GS} = V_{DC} + v_{ac} = V_{GS} + v_{gs}$$

$$i_D = k(v_{GS} - V_t)^2 = k(V_{GS} + v_{gs} - V_t)^2 \Rightarrow$$

$$i_D = k(V_{GS} - V_t)^2 + 2k(V_{GS} - V_t)v_{gs} + k v_{gs}^2$$

let $k v_{gs}^2 \ll 2k(V_{GS} - V_t) v_{gs} \Rightarrow v_{gs} \ll 2(V_{GS} - V_t) \Rightarrow |v_{gs}|_{max} \cong 0.2(V_{GS} - V_t)$

This is called the small signal approximation. This must hold For all the derivations after this point.

We, now, have

$$i_D \cong \underbrace{k(V_{GS} - V_t)^2}_{\parallel} + 2k(V_{GS} - V_t)v_{gs} \Rightarrow$$

$I_D$

From The DC problem

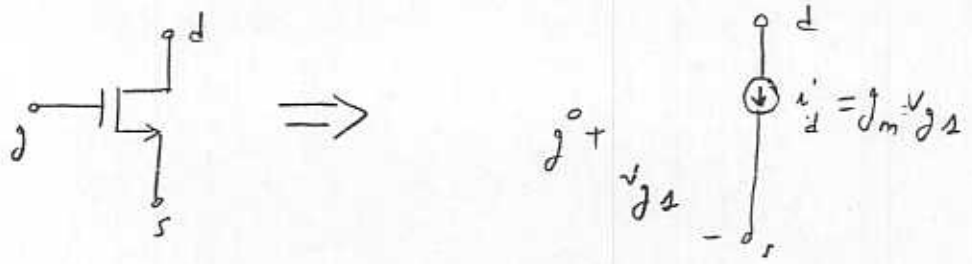
$$i_D = I_D + \underbrace{2k(V_{GS} - V_t)}_{g_m} v_{gs} \Rightarrow i_D = I_D + g_m v_{gs} = I_D + i_d$$

$g_m$ transconductance

$$\Rightarrow i_d = g_m v_{gs}$$

This means that again $i_D$ has two components. The DC component $I_D$ is generated From the DC supplies which also place the MOSF in Pinch oFF. The AC component $i_d = g_m v_{gs}$ is generated From the Ac supply. The Ac component $i_d = g_m v_{gs}$ assumes that the small signal approximation $\left[|v_{gs}| \ll 2k(V_{GS} - V_t) \text{ or } |v_{gs}|_{max} \cong 0.2k(V_{GS} - V_t)\right.$ holds.

The AC model of a MOSFET is, therefore, given by




Note that gate is open because $i_g = 0$.

Approach to solving MOSFET amplifier problems:
Use superposition.

1) First kill the AC supplies. Assume pinch off. Find $V_{GS}$, $I_D$ and $V_{DS}$. Verify the inequalities associated with pinch off. Compute the AC model parameter $g_m = 2k(V_{GS} - V_t)$ which depends on the DC voltage $V_{GS}$

2) kill the DC supplies. Replace the MOSFET with its AC model. Find the AC quantities $v_{gs}$, $i_d$ and $v_{ds}$. Verify the small signal approximation $|v_{gs}| \ll 2(V_{GS} - V_t)$ holds. This guarantees that the AC model is valid.

3) Find the total voltage and current signals from

$$v_{GS} = V_{GS} + v_{gs}$$

$$i_D = I_D + i_d$$

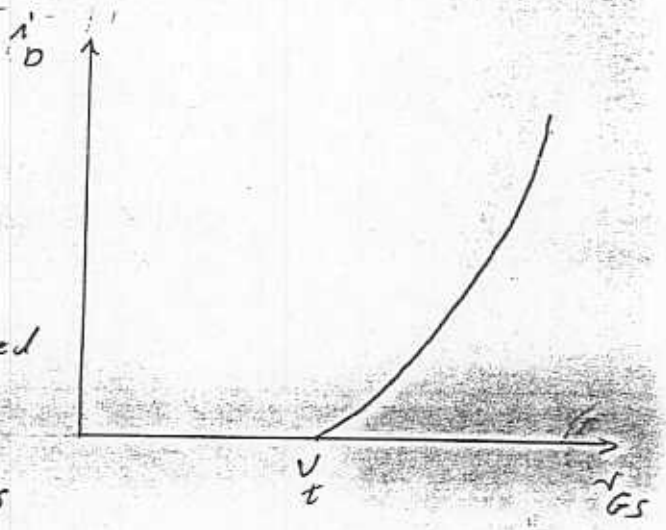
$$v_{DS} = V_{DS} + v_{ds}$$

Note that in many amplifier problems, the quantities of interest may be voltage and current gains, and input and output resistances which are obtained from the AC circuit.

Another approach to Find $g_m$:

For pinch-off, we have $i_D = k(v_{GS} - V_t)^2$.

The DC circuit establishes a DC operating point ($V_{GS}$, $I_D$, $V_{DS}$) as shown below.




Now, if an AC supply $v_{gs}$ is superimposed on top of the DC (voltage $V_{GS}$), it causes small changes in total $v_{GS}$ about the DC $V_{GS}$. For small changes about $V_{GS}$, the $i_D$ - $v_{GS}$ curve has the slope:

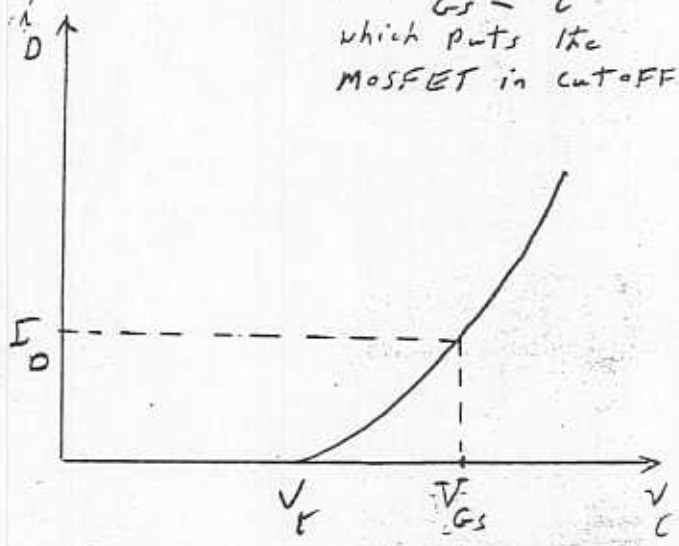
$$\left.\frac{\partial i_D}{\partial v_{GS}}\right|_{\substack{\text{about} \\ V_{GS}}} = \left. 2k(v_{GS} - V_t)\right|_{\text{at } V_{GS}}$$

$$= 2k(V_{GS} - V_t) = g_m$$

This shows how the MOSFET reacts to small ac $v_{gs}$ about a DC $V_{GS}$. This is the same value of $g_m$ derived before.

1) $v_{GS} > V_t$ to be in pinch off

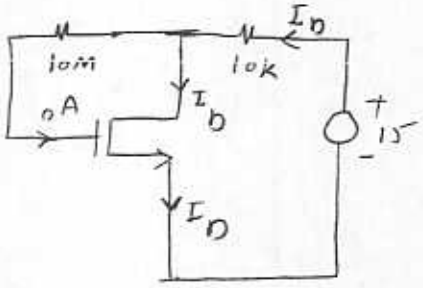
2) Note that $i_D = 0$ For $v_{GS} \leq V_t$ which puts the MOSFET in cut-off

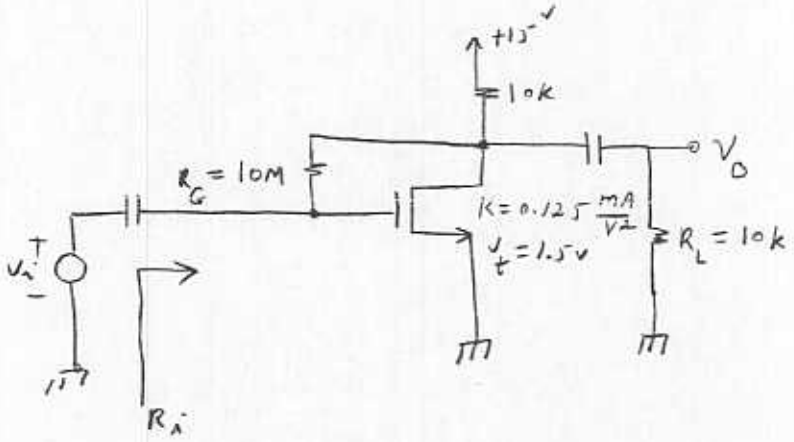



range of total voltage $v_{GS}$

Ex. Consider the circuit shown below.

a/ DC Problem:




Assume pinch off:

$$\begin{cases} I_D = 0.125\times10^{-3}(V_{GS}-1.5)^2 & ① \\ -15+10kI_D+10M(0)+V_{GS}=0 \Rightarrow I_D = \dfrac{15-V_{GS}}{10k} \end{cases}$$

$$① \Rightarrow \frac{15-V_{GS}}{10k} = 0.125\times10^{-3}(V_{GS}-1.5)^2 \Rightarrow V_{GS} = -2.208,\ 4.408$$

we need $V_{GS} > V_t = 1.5 \Rightarrow$ choose $V_{GS} = 4.408 \Rightarrow$

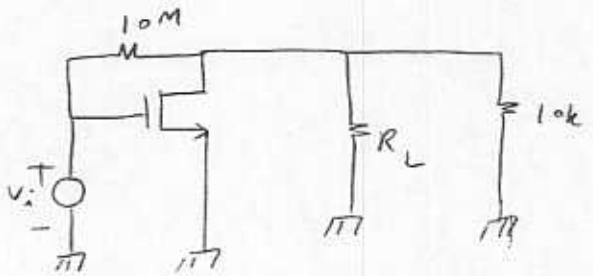
$$I_D = \frac{15-4.408}{10k} = 1.06\ mA$$

$$KVL \Rightarrow -15+10kI_D+V_{DS}=0 \Rightarrow V_{DS} = 4.4 \geq V_{GS}-V_t = 4.408-1.5 = 2.908\ \checkmark$$

$$g_m = 2k(V_{GS}-V_t) = 2\times0.125\times10^{-3}(4.408-1.5) = 0.725\times10^{-3}\ A/V$$

b/ $V_o/V_i$:

AC circuit:

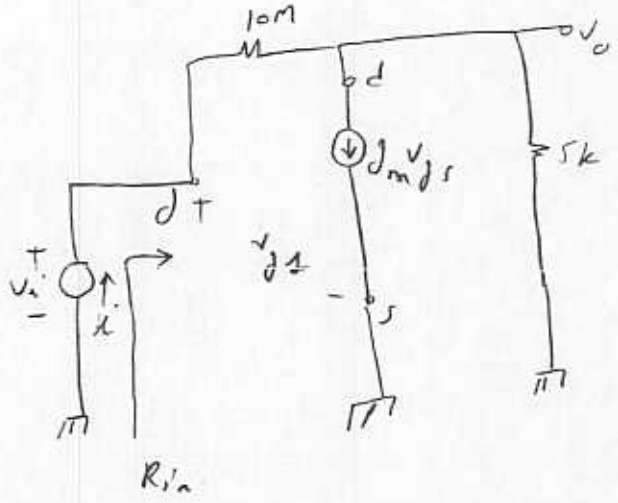


KCL $\Rightarrow \frac{V_o - V_i}{10M} + g_m V_{gs} + \frac{V_o}{5k} = 0$ ①

KVL $\Rightarrow -V_i + V_{gs} = 0 \Rightarrow V_i = V_{gs}$

① $\Rightarrow \frac{V_o - V_i}{10^7} + 0.725\times10^{-3} V_i + \frac{V_o}{5k} = 0 \Rightarrow$

$\frac{V_o}{V_i} = -3.625$




c/ $R_{in}$:

$R_{in} = \frac{V_i}{i}$

$i = \frac{V_i - V_o}{10M} = \frac{V_i + 3.625 V_i}{10M}$

$R_{in} = \frac{V_i}{i} = \frac{V_i}{\frac{4.625 V_i}{10M}} = 2.16M$ This is a huge $R_{in}$!

d/ Find all values of $V_i$ for small signal approximation to hold:

$|V_{gs}| \leq 0.2(V_{GS} - V_t) = 0.2(4.408 - 1.5) = 0.5816$

The biggest $V_{gs}$ can be $V_{gs}(t) = 0.5816 \Rightarrow V_i(t) = 0.5816 \sin 2\pi F t$

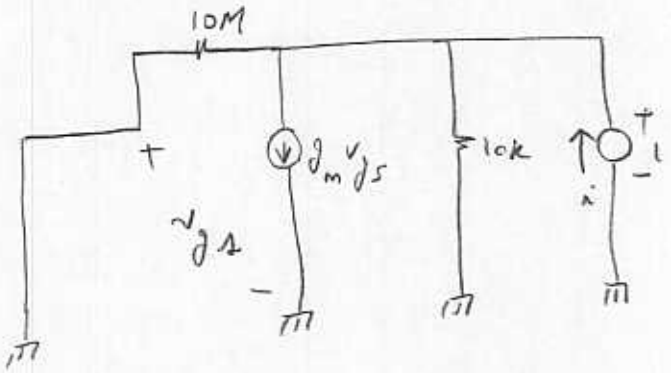
e/ $R_{out}$ excluding $R_L$:

KVL $\Rightarrow V_{gs} = 0$

KCL $\Rightarrow \frac{1}{10M} + g_m V_{gs} + \frac{1}{10k} - i = 0 \Rightarrow$

$i = \frac{1}{10M} + \frac{1}{10k} \Rightarrow$

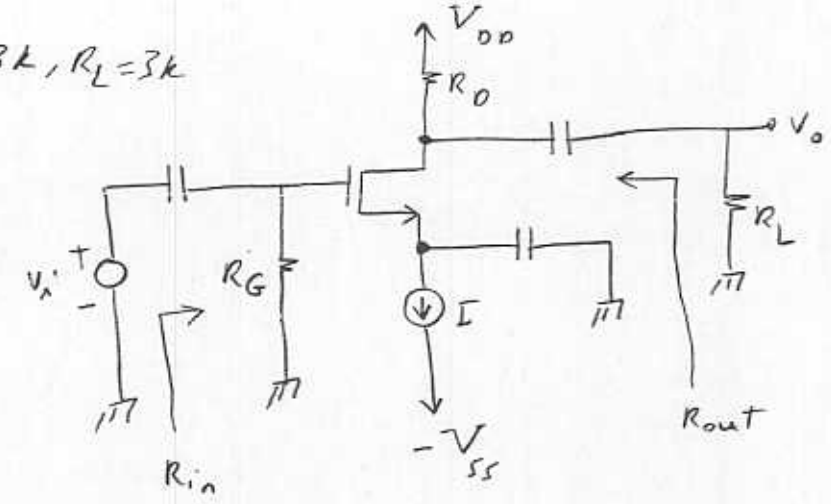
$R_{out} = 10M \,||\, 10k \cong 10k$



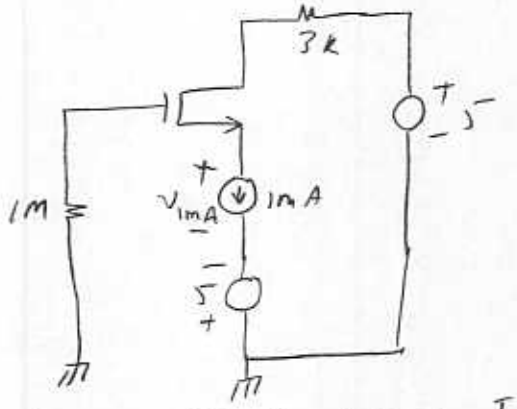
Common-source amplifier:

let $I = 1mA$, $k = 1mA/V^2$, $V_t = 1^V$

$V_{DD} = V_{SS} = 5$, $R_G = 1M$, $R_D = 3k$, $R_L = 3k$




a/ DC problem:




Assume pinch off $\Rightarrow I_D = 10^{-3}(V_{GS} - 1)^2 \Rightarrow$

$10^{-3} = 10^{-3}(V_{GS} - 1)^2 \Rightarrow V_{GS} - 1 = \pm 1 \Rightarrow V_{GS} = 0, 2$

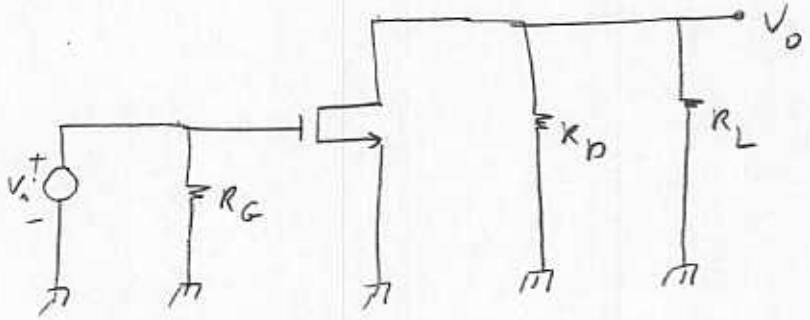
we need $V_{GS} > V_t = 1 \Rightarrow$ choose $V_{GS} = 2^V$.

$KVL \Rightarrow 1M(0) + V_{GS} + V_{1mA} - 5 = 0 \Rightarrow V_{1mA} = 5 - V_{GS} = 3^V$

$KVL \Rightarrow -5 + 3k(1m) + V_{DS} + 3 - 5 = 0 \Rightarrow V_{DS} = 4 \geq V_{GS} - V_t = 2 - 1 = 1$ ✓

$g_m = 2k(V_{GS} - V_t) = 2 \times 10^{-3}(2-1) = 2mU$

b/ $V_o/V_i$:

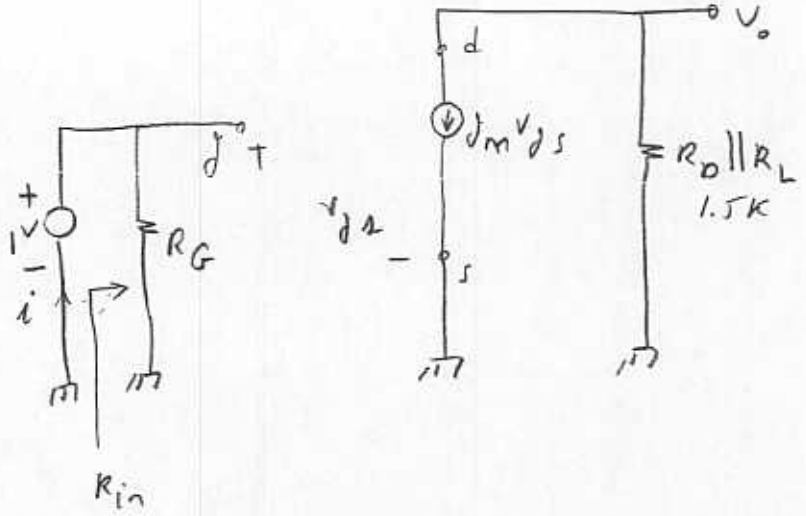



Note that source is grounded in the AC problem $\Rightarrow$ common-source amplifier

$V_o = -1.5k\, g_m V_{gs} = -3 V_{gs}$

$KVL \Rightarrow -V_i + V_{gs} = 0 \Rightarrow V_{gs} = V_i$

$\frac{V_o}{V_i} = -3$

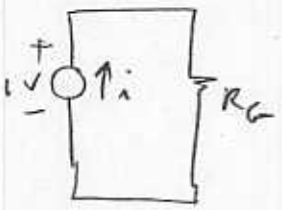



**$R_{in}$:**

$i = \frac{1}{R_G} \Rightarrow$

$R_{in} = \frac{1}{i} = R_G = 1M$



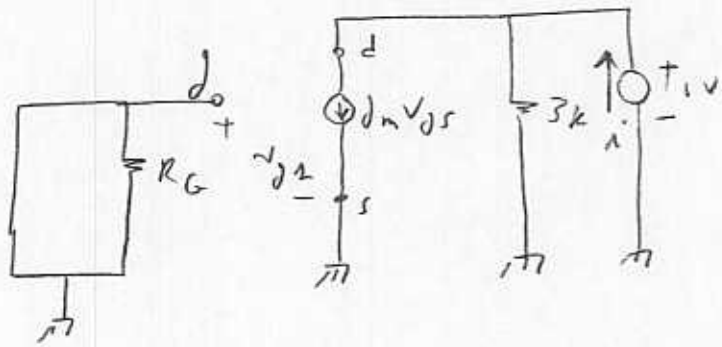




**$R_{out}$:**

$KVL \Rightarrow V_{gs} = 0$

$KCL \Rightarrow g_m V_{gs} + \frac{1}{3k} - i = 0 \Rightarrow$

$i = \frac{1}{3k} \Rightarrow R_{out} = 3k$




For a common-source amplifier, we have (in terms of circuit variables)

$A_V = \frac{V_o}{V_i} = -g_m (R_L \| R_D)$

$R_{in} = R_G$

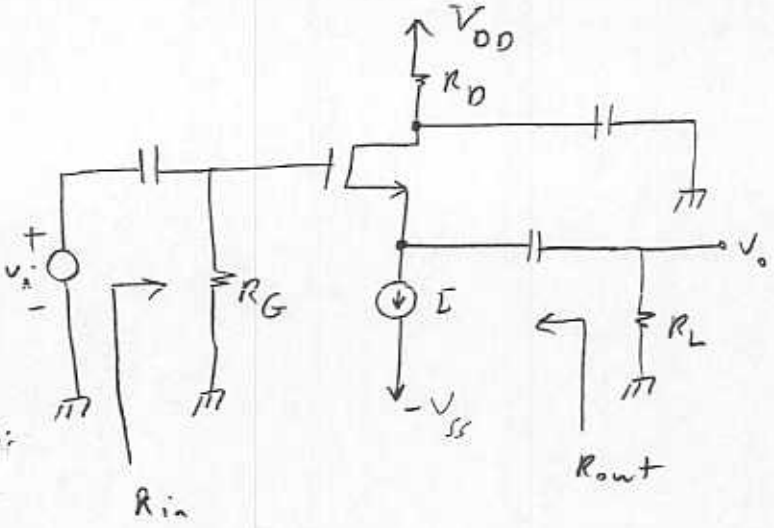
$R_{out} = R_D$

# Common-Drain amplifier or Source Follower:

let $I = 1mA$, $k = 1mA/V^2$

$V_t = 1$, $V_{DD} = V_{SS} = 5$

$R_G = 1M$, $R_D = 3k$, $R_L = 3k$



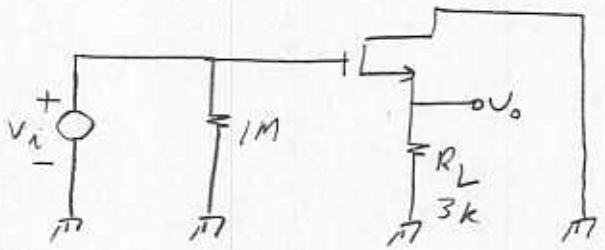

a/ DC problem:
exactly the same as the previous problem:

$V_{GS} = 2$, $I_D = 1mA$, $V_{DS} = 4$

$g_m = 2mV$

b/ $V_o/V_i$

$V_o = 3k\, g_m V_{gs} = 6 V_{gs}$




KVL $\Rightarrow -V_i + V_{gs} + V_o = 0$

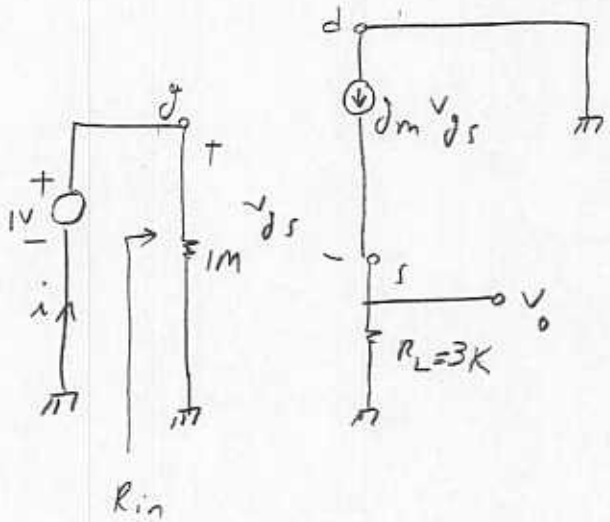
$\Rightarrow \frac{V_o}{V_i} = \frac{6V_{gs}}{V_{gs} + 6V_{gs}} = \frac{6}{7} < 1$ ?

Note that drain is grounded in the AC problem $\Rightarrow$ Common drain amplifier

c/ $R_{in} = \frac{1}{i}$

$i = 1/1M \Rightarrow$

$R_{in} = R_G = 1M$

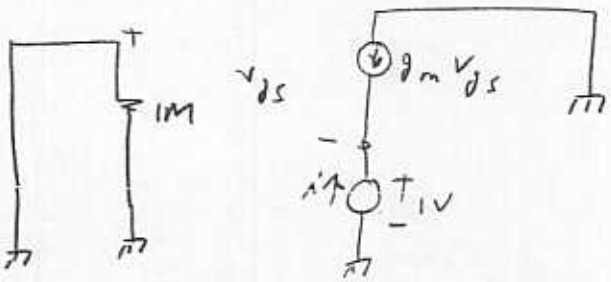


d/ $R_{out}$ excluding $R_L$:

KVL $\Rightarrow 0 + V_{gs} + 1 = 0 \Rightarrow V_{gs} = -1$

$i = -g_m V_{gs} = g_m = 2 \times 10^{-3}$

$R_{out} = \frac{1}{i} = 500\,\Omega$ small $R_{out}$!




For a common-drain amplifier, we have (in terms of circuit variables)

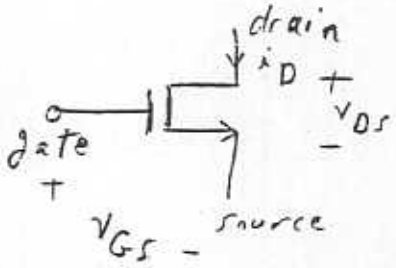
$$A_v = \frac{V_o}{V_i} = \frac{R_L}{R_L + \frac{1}{g_m}}$$ close to 1

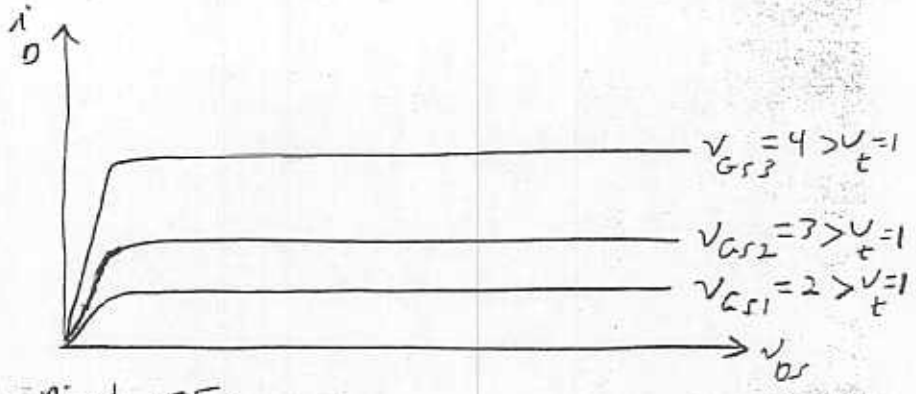
$R_{out} = \frac{1}{g_m}$ small

$R_{in} = R_G$ large

} behavior similar to a CC amplifier

So far, we have covered enhancement MOSFETs.




Pinch off:

$$i_D = K(v_{GS} - V_t)^2, \quad v_{GS} > V_t > 0, \quad v_{DS} \geq v_{GS} - V_t$$

triode:

$$i_D = K\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right], \quad v_{GS} > V_t > 0,$$

$$v_{DS} \leq v_{GS} - V_t$$

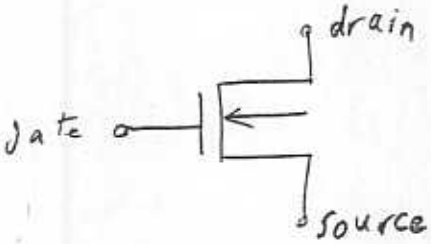
Cut off:

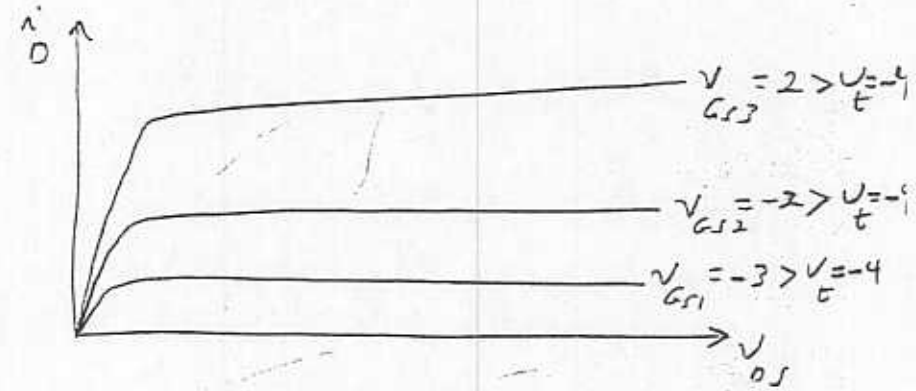
$$i_D = 0, \quad v_{GS} \leq V_t$$

Note that for an enhancement MOSFET, we have $V_t > 0$. For example, in the graph shown above we have $V_t = 1$ V.

For a depletion type MOSFET, all the equations and graphs shown above holds. For a depletion type MOSFET, however, $V_t$ is less than zero.

Ex. If $V_t = -4$ V for a depletion type n-channel MOSFET, we have



Pinch oFF: ($V_t = -4$)

$i_D = k(v_{GS}+4)^2$, verify $v_{GS} > -4$ and $v_{DS} \geq v_{GS}+4$

triode:

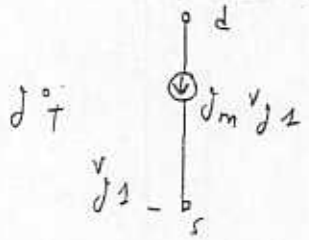
$i_D = k[2(v_{GS}+4)v_{DS} - v_{DS}^2]$, verify $v_{GS} > -4$ and $v_{DS} \leq v_{GS}+4$

cut oFF:

$i_D = 0$, $v_{GS} \leq -4$.

Since the i-v equations are identical to enhancement type n-channel MOSFET, the AC model is given by

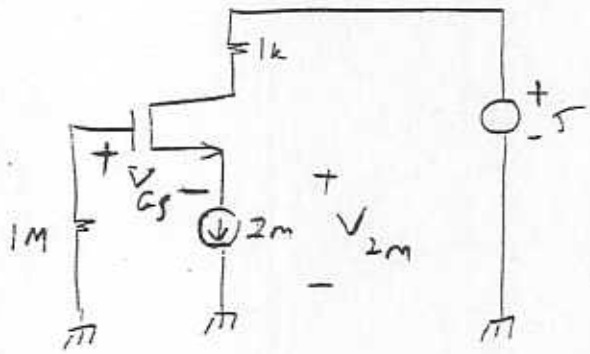
$g_m = 2k(V_{GS} - V_t)$

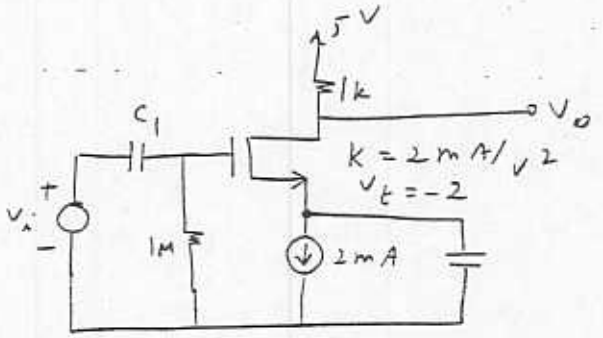



Ex.

a/ DC Analysis:

Assume pinch oFF




$I_D = K(V_{GS} - V_t)^2 \Rightarrow 2m = 2m(V_{GS}+2)^2 \Rightarrow (V_{GS}+2)^2 = 1 \Rightarrow V_{GS}+2 = \pm 1 \Rightarrow$

$V_{GS} = -1, -3$ choose $V_{GS} = -1 > V_t = -2$ ✓

KVL $\Rightarrow$ $1M(0) + V_{GS} + V_{2m} = 0 \Rightarrow V_{2mA} = -V_{GS} = 1$

KVL $\Rightarrow$ $-5 + 1k(2m) + V_{DS} + 1 = 0 \Rightarrow V_{DS} = 2 \geq V_{GS} - V_t = -1 - (-2) = 1$ ✓

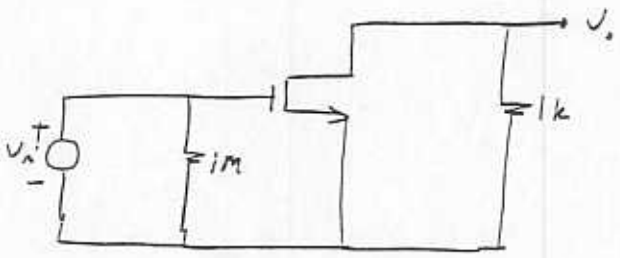
$g_m = 2k(V_{GS} - V_t) = 2 \times 2 \times 10^{-3}(-1+2) = 4mU$

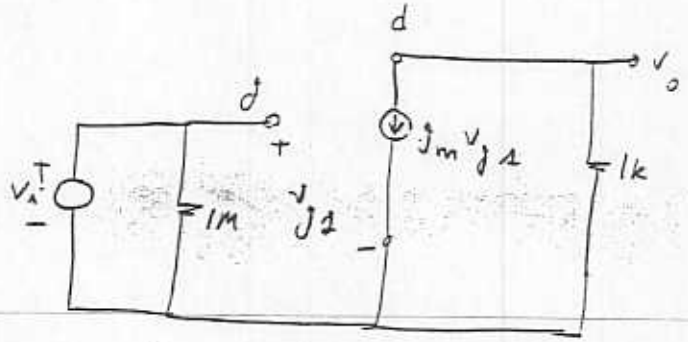
b/ $v_o/v_i$ :

KVL $\Rightarrow -v_i + v_{gs1} = 0$

$v_o = -1k\, g_m v_{gs} = -4 v_{gs1}$

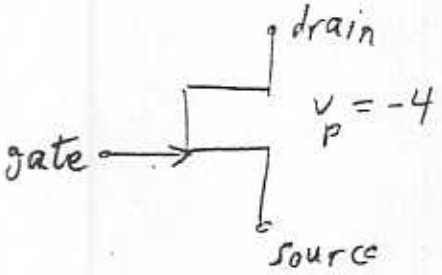
$v_o/v_i = \dfrac{-4v_{gs1}}{v_{gs1}} = -4$

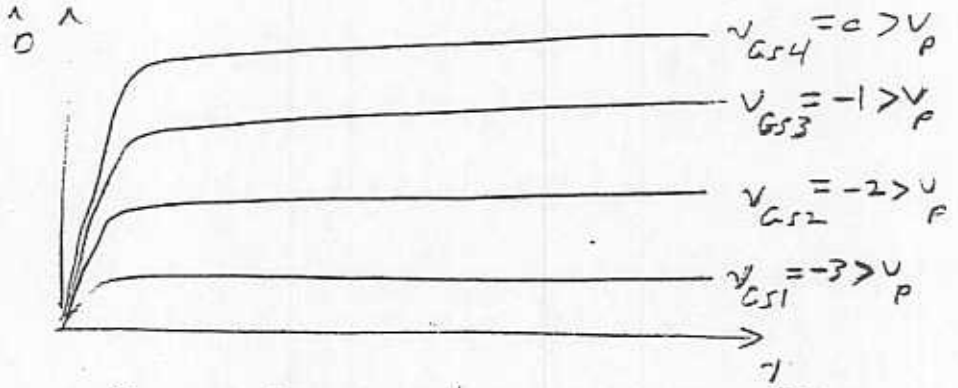



Junction Field-Effect Transistor (JFET):

A JFET is very similar to a depletion type MOSFET. A JFET also has a negative value of $v_t$, $v_t$ (Threshold voltage) for a JFET is called Pinch-off voltage and is represented by $v_p$.




For a JFET, values of $v_{GS}$ above zero are not allowed.

Note that for a depletion MOSFET, values of $v_{GS}$ above zero are allowed as shown on Page 1.

JFET and depletion MOSFET both have negative threshold voltages. JFET does not allow values of $v_{GS}$ above zero but depletion MOSFET

does.

pinch-off:

$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2$, verify $v_{GS} > V_p$ and $v_{DS} \geq v_{GS} - V_p$

$I_{DSS}$ and $V_p$ are both specified by the manufacturer.

triode:

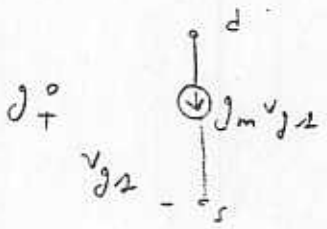
$i_D = I_{DSS}\left[2\left(1 - \frac{v_{GS}}{V_p}\right)\left(\frac{v_{DS}}{-V_p}\right) - \left(\frac{v_{DS}}{V_p}\right)^2\right]$, verify $v_{GS} > V_p$ and $v_{DS} \leq v_{GS} - V_p$

cut off:

$i_D = 0$, $v_{GS} \leq V_p$

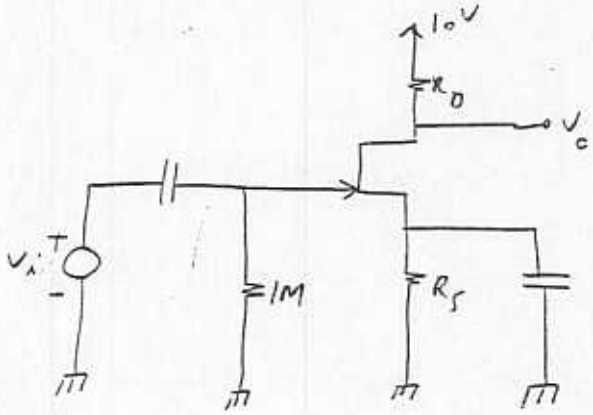
AC model of JFETs.

$g_m = \frac{2 I_{DSS}}{|V_p|}\sqrt{\frac{I_D}{I_{DSS}}}$

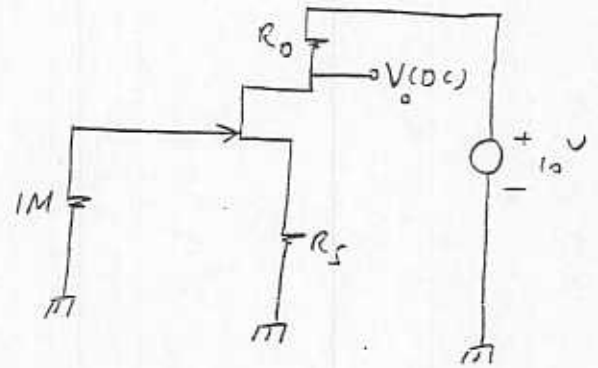



note that $g_m$ depends on the DC quantity $I_D$.

Ex. let $V_p = -4$, $I_{DSS} = 16\,mA$.
Find $R_D$ and $R_S$ such that $I_D = 4\,mA$ and $V_D(DC) = 6\,V$.



a/ DC Problem:




Assume pinch-off.

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \Rightarrow$

$4m = 16m\left(1 - \frac{V_{GS}}{-4}\right)^2 \Rightarrow$

$\left(1 + \frac{V_{GS}}{4}\right)^2 = \frac{1}{4} \Rightarrow 1 + \frac{V_{GS}}{4} = \pm\frac{1}{2} \Rightarrow$

$V_{GS} = -2, -6$ choose $V_{GS} = -2 > V_p = -4$

KVL $\Rightarrow -10 + R_D(4m) + 6 = 0 \Rightarrow R_D = 1k$

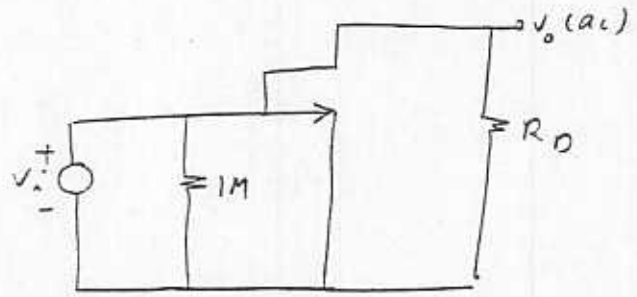
KVL $\Rightarrow 1M(0) + V_{GS} + R_S I_D = 0 \Rightarrow -2 + R_S(4m) = 0 \Rightarrow R_S = 0.5k$

KVL $\Rightarrow -10 + 1k(4m) + V_{DS} + 0.5k(4m) = 0 \Rightarrow V_{DS} = 4 \geq V_{GS} - V_p = -2 - (-4) = 2V$

$g_m = \frac{2I_{DSS}}{|V_p|}\sqrt{\frac{I_D}{I_{DSS}}} = \frac{2(16m)}{4}\sqrt{\frac{4m}{16m}} = 8m\sqrt{1/4} = 4m$

b/ AC problem:

$V_o/V_i$:



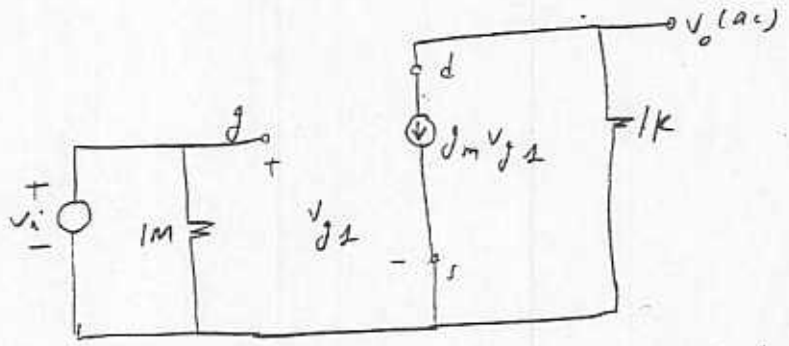

$V_o = -1k\, g_m V_{gs} = -4V_{gs}$

KVL $\Rightarrow -V_i + V_{gs} = 0$

$\frac{V_o}{V_i} = -4$

$R_{in}$:

$R_{in} = 1M$




Note that the AC problem looks like the common-source amplifier analysed for the enhancement type n-channel MOSFET in handout # 22. The AC equations derived in that handout apply here.

Handout #24

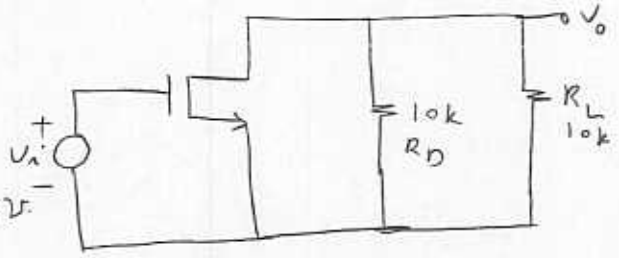
Ex. Consider the MOSFET shown.

The AC circuit is shown.

Assume DC analysis has given

$V_{GS} = 4,\ V_{DS} = 5^V$

$g_m = 2k(V_{GS} - V_t) = 2\times 10^{-3}(4-3) = 2mS$




$k = 10^{-3}\ A/V^2$

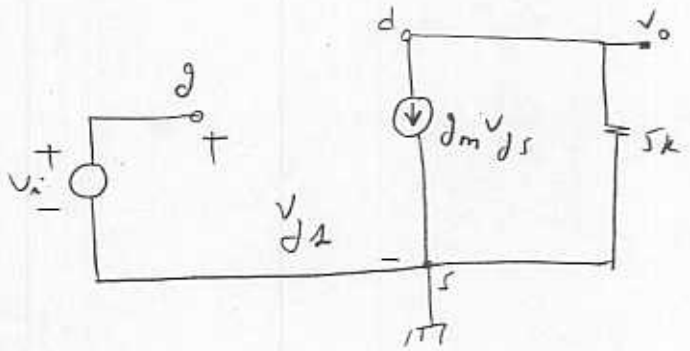
$V_t = 3^V$

a/ Find $v_o/v_i$.

$V_o = -5k\, g_m V_{gs}$

KVL $\Rightarrow -v_i + V_{gs} = 0 \Rightarrow$

$v_o/v_i = -5k\, g_m = -10$




b/ Find all $v_i$ for SSA to hold.

$|v_{gs}| \le 0.2(V_{GS} - V_t)$ Do not forget the magnitude sign!

$\Rightarrow |V_{gs}| = |V_i| \le 0.2(4-3) = 0.2 \Rightarrow \quad -0.2 \le V_i \le 0.2$

c/ Find all $v_i$ for the MOSFET to avoid cutoff.

Two ways to do:

1) To avoid cutoff ($V_{GS} \le V_t$), make sure you keep

$V_{GS} = V_{GS} + v_{gs} > V_t \Rightarrow 4 + v_i \ge 3 \Rightarrow \underline{V_i \ge -1}$

2) Make sure $i_D = I_D + i_d \ge 0 \Rightarrow$

$I_D = k(V_{GS} - V_t)^2 = 10^{-3}(4-3)^2 = 1mA$

$1m + g_m v_{gs} \geq 0 \Rightarrow 1m + 2\times10^{-3} v_i \geq 0 \Rightarrow \underline{v_i \geq -0.5}$

Both ① and ② are conditions we can use for cutoff. We should take the one that satisfies both.

$$\underline{V_i \geq -0.5}$$

In other words, take the tighter condition.

d/ Find all $v_i$ for MOSFET to avoid triode.

We get to triode when $v_{DS} \leq v_{GS} - v_t$.

Make sure $v_{DS} \geq v_{GS} - v_t \Rightarrow$

$V_{DS} + v_{ds} \geq V_{GS} + v_{gs} - V_t \Rightarrow$

$5 + v_o \geq 4 + v_i - 3 \Rightarrow 5 - 10 v_i \geq 4 + v_i - 3 \Rightarrow 11 v_i \leq 4$

$v_i \leq 0.36\ V$

e/ Find $v_i$ such that a reliable amplifier is obtained.

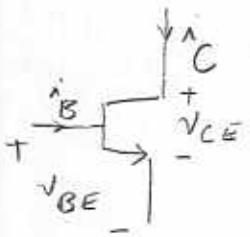
Make sure SSA and avoiding cutoff and triode are all achieved.

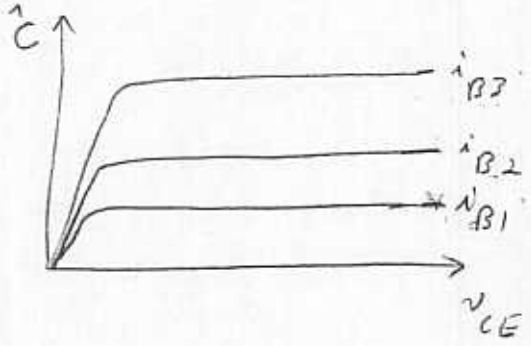
$$\left.\begin{aligned} -0.2 \leq v_i \leq 0.2 \\ -0.5 \leq v_i \\ v_i \leq 0.36 \end{aligned}\right\} \Rightarrow \quad -0.2 \leq v_i \leq 0.2$$

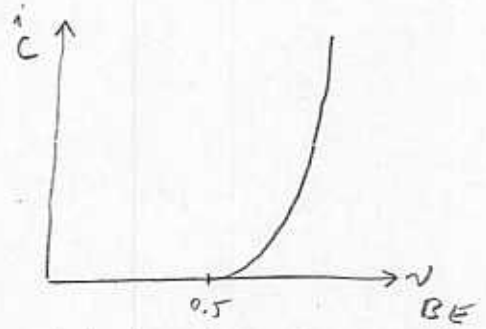
$\Rightarrow v_i$ can be $\underline{v_i(t) = 0.2 \sin \omega t}$

loose ends of BJTs and FETs (MOSFETs or JFETs):

1) BJTs:



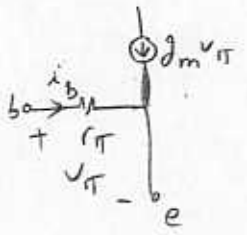




$i_C \perp v_{BE}$ in active region

In active region, we have $i_C = I_S e^{v_{BE}/V_T}$ independent of $v_{CE}$. From this equation, we derived the AC model of the BJT.

$$\begin{cases} i_c = g_m v_\pi \\ i_b = v_\pi / r_\pi \end{cases}$$

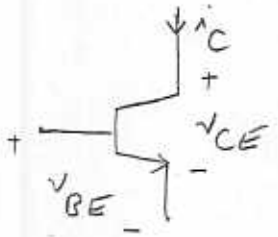



Note that $i_c = g_m v_\pi = g_m v_{be}$ does not depend on $v_{CE}$ because total $i_C = I_S e^{v_{BE}/V_T}$ does not depend on $v_{CE}$

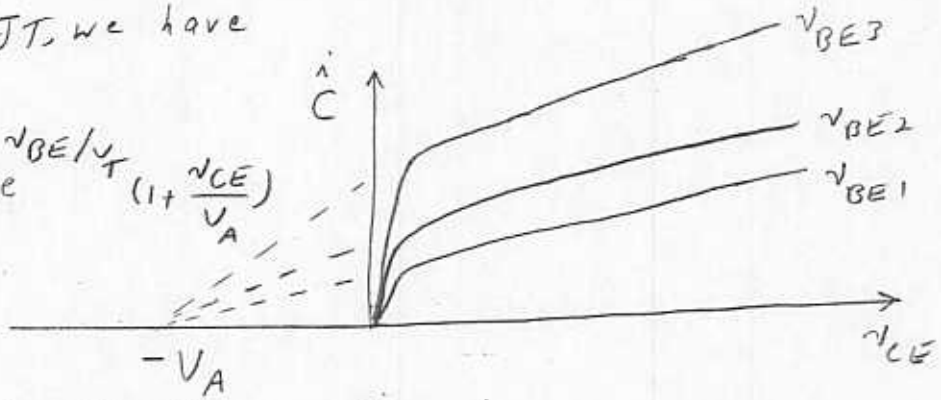
In the active region, $i_C$ does not change as a function of $v_{CE}$

All the equation shown above are true for an <u>ideal</u> BJT

For a real-life BJT, we have

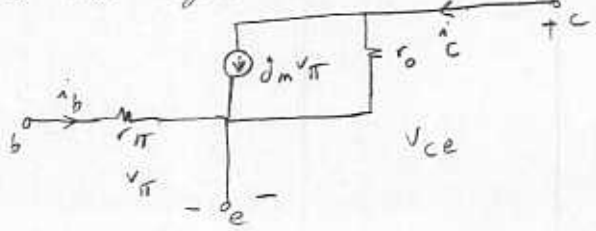



$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$




The AC model derived with this equation is

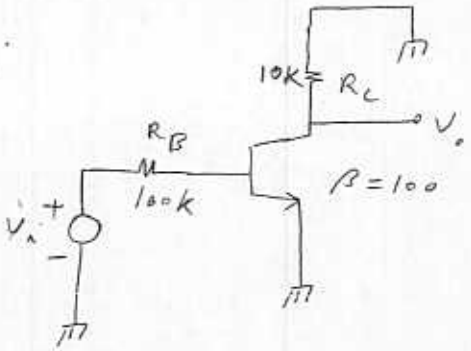
$$\begin{cases} i_c = g_m v_\pi + v_{ce}/r_o \\ i_b = v_\pi / r_\pi \end{cases} \Rightarrow$$




$$r_o \triangleq \frac{V_A}{I_C}$$

Ex. Consider the AC circuit shown.

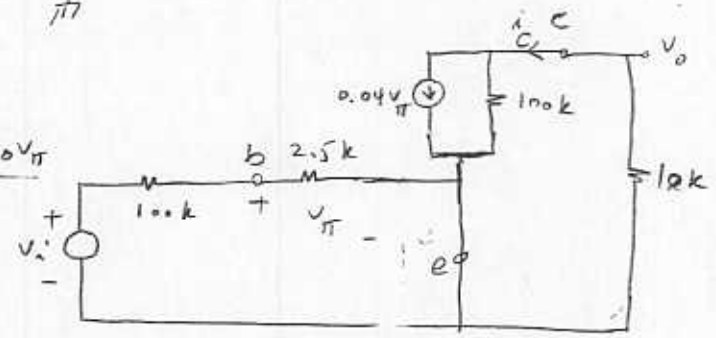
Let $I_C = 1mA$, $V_A = 100V$. Find $v_o/v_i$.




$$g_m = \frac{I_C}{V_T} = \frac{1mA}{25mV} = 0.04$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{0.04} = 2.5k$$

$$r_o = \frac{V_A}{I_C} = \frac{100}{1m} = 100k$$




$$\begin{cases} \text{KCL} \Rightarrow 0.04v_\pi + \frac{v_o}{100k} + \frac{v_o}{10k} = 0 \Rightarrow v_o = -\frac{4000v_\pi}{11} \\ v_\pi = \frac{2.5k}{100k + 2.5k} v_i \end{cases}$$

$$\Rightarrow \frac{v_o}{v_i} = \frac{\frac{-4000}{11} v_\pi}{\frac{102.5}{2.5} v_\pi} = -8.87 \quad \text{if } r_o = \infty \text{ (ideal BJT)} \Rightarrow \frac{v_o}{v_i} = -9.75$$

You can also find AC quantities such as $R_{in}$ and $R_{out}$ from this real-life AC model.

It is usually a good approximation to drop $r_o$ from the AC model and use the ideal AC model. The only time you want to use the real-life AC model is when you are specifically asked to.

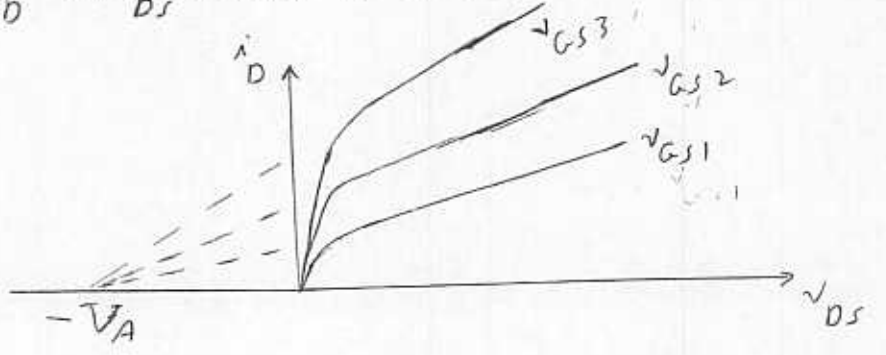
2) Real-life FETs:

For an ideal MOSFET or JFET $\Rightarrow i_D = K(v_{GS} - v_t)^2$ or $i_D = I_{DSS}(1 - \frac{v_{GS}}{v_p})^2$ independent of $v_{DS}$ in the flat portion of the curve. In reality,

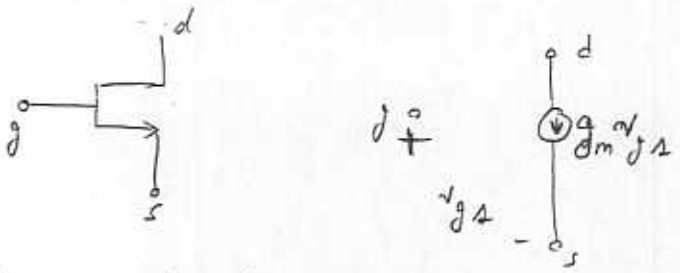
MOSFET in pinch-off:
$$i_D = K(v_{GS} - v_t)^2(1 + \lambda v_{DS})$$

JFET in pinch-off
$$i_D = I_{DSS}(1 - \frac{v_{GS}}{v_p})^2(1 + \lambda v_{DS})$$

Tipically, we have $0.005 \leq \lambda \leq 0.03$. $\lambda$ determines the degree of dependence of $i_D$ on $v_{DS}$ which is a measure of how non-ideal the FET is.



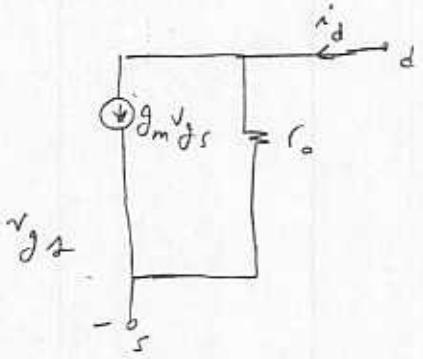
For the ideal FET, the Ac model obtained from $i_D = k(V_{GS} - V_t)^2$ or $i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ is




For the non-ideal FET, From the equations shown on the last page, we obtain

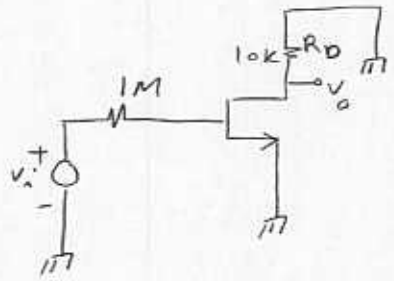
$$i_d = g_m v_{gs} + v_{ds}/r_o$$

where $r_o \cong \frac{V_A}{I_D}$.




Ex. Consider the AC circuit shown below.

Let $I_D = 1mA$, $g_m = 4mV$ and $V_A = 100$.




a/ $v_o/v_i$:

$r_o = \frac{V_A}{I_D} = 100k$

KCL $\Rightarrow g_m v_{gs} + \frac{v_o}{100k} + \frac{v_o}{10k} = 0 \Rightarrow v_o = \frac{-400 v_{gs}}{11}$

KVL $\Rightarrow -v_i + 1M(0) + v_{gs} = 0 \Rightarrow v_i = v_{gs}$

$v_o/v_i = -\frac{400}{11} = -36.36$ ($r_o = \infty \Rightarrow \frac{v_o}{v_i} = -40$)

b/ $R_{in}$ seen by $v_i$:

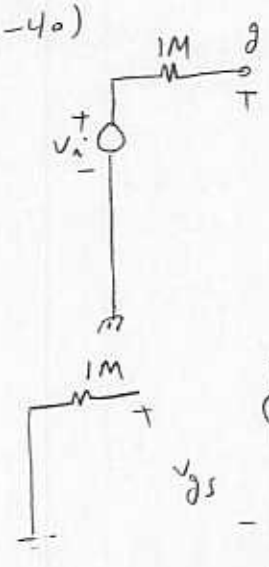
Apply a 1V $\Rightarrow R_{in} = \frac{1}{i}$

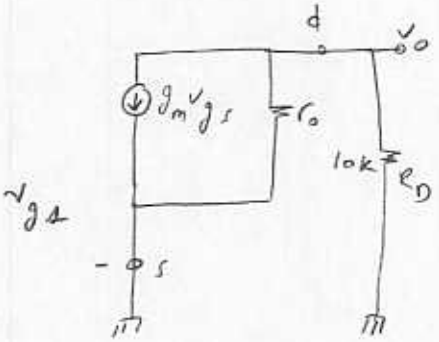
$i = 0 \Rightarrow R_{in} = \infty$

c/ $R_{out}$: $v_{gs} = 0 \Rightarrow$

$R_{out} = 10k \,//\, 100k = 9.09k$

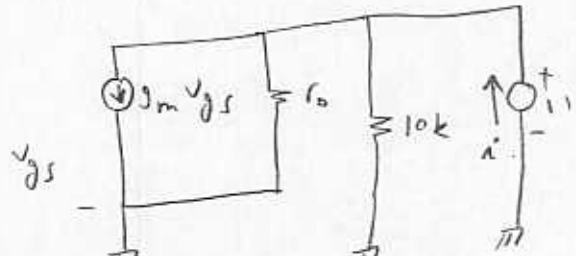
Why is $R_{out} = 10k \,//\, 100k$.









# ENGR.364
## Handout #25

1) An example of a problem that can be designed with logic circuits: we want to launch a missle. The decision to launch is partly under the control of a launch officer (called C), who signifies a launch-ready condition by throwing a switch. We do not trust the launch officer entirely, so we assign two other individuals (A and B) to help him. A and B also have switches to signify launch-ready condition, but we give them less authority than the launch officer. IF either A or B signifies a launch-ready condition and the launch officer also signifies a launch-ready condition, then we have a launch-ready condition. To design a logic circuit that will perform the function described above, we first express the function as an equation.

$$L = (A \text{ or } B) \text{ and } C$$

our task in this course is to design an electronic circuit that will perform the operations of the equation.

Boolean Algebra:

In boolean algebra, all variables and relations are two-valued. IF A is a boolean variable, then

$A = 1$ means A is true or asserted

$A = 0$ means A is False or not-asserted

There are three basic operations in boolean algebra.

not: symbolized by an overbar. not is also called the complement.

| $A$ | $\bar{A}$ |
|---|---|
| 0 | 1 |
| 1 | 0 |

$\bar{A}$ is the complement of $A$.

$\bar{1} = 0$ , $\bar{0} = 1$

and: $A$ and $B = A \cdot B = AB$

| $A$ | $B$ | $A \cdot B$ |
|---|---|---|
| 0 | 0 | $0 \cdot 0 = 0$ |
| 0 | 1 | $0 \cdot 1 = 0$ |
| 1 | 0 | $1 \cdot 0 = 0$ |
| 1 | 1 | $1 \cdot 1 = 1$ |

$A \cdot B$ is 1 only if both $A$ and $B$ are 1.

or: $A$ or $B = A + B$

| $A$ | $B$ | $A + B$ |
|---|---|---|
| 0 | 0 | $0 + 0 = 0$ |
| 0 | 1 | $0 + 1 = 1$ |
| 1 | 0 | $1 + 0 = 1$ |
| 1 | 1 | $1 + 1 = 1$ |

$A + B$ is 1 if either $A$ or $B$ is one.

Some relationships to think about:

| and | or |
|---|---|
| $0 \cdot A = 0$ | $1 + A = 1$ |
| $1 \cdot A = A$ | $0 + A = A$ |
| $A \cdot A = A$ | $A + A = A$ |
| $A \cdot \bar{A} = 0$ | $A + \bar{A} = 1$ |

The following identities hold:

$A + B = B + A$, $AB = BA$, $A(B + C) = AB + AC$

$A + BC = (A + B)(A + C) = A \cdot A + AC + BA + BC = A + BA + BC = A(1 + B) + BC$
$= A + BC$

Some Practice with boolean algebra:

Prove $A + AB = A$ $\quad A + AB = A \cdot 1 + AB = A(1 + B) = A$

Prove $A(A + B) = A$ $\quad A(A+B) = AA + AB = A + AB = A \cdot 1 + AB = A(1+B) = A \cdot 1 = A$

Prove $AB + A\bar{B} = A$ $\quad AB + A\bar{B} = A(B + \bar{B}) = A(1) = A$

Prove $(A+B)(A+\bar{B}) = A$ $\quad (A+B)(A+\bar{B}) = AA + A\bar{B} + BA + B\bar{B} =$

$A + A\bar{B} + AB + 0 = A(1+\bar{B}) + AB =$

$A + AB = A(1+B) = A$

DeMorgan's Theorem:

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

Proof: $\overline{A+B} = \bar{A} \cdot \bar{B}$

| A | B | $A+B$ | $\overline{A+B}$ | $\bar{A}$ | $\bar{B}$ | $\bar{A} \cdot \bar{B}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Compare

$$\overline{AB + AC} = (\overline{AB}) \cdot (\overline{AC}) = (\bar{A} + \bar{B}) \cdot (\bar{A} + \bar{C})$$

$$\overline{(A+B) \cdot (A+C)} = \overline{(A+B)} + \overline{(A+C)} = \bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C}$$

$$\overline{A + BC} = \overline{A + (BC)} = \bar{A} \cdot \overline{(BC)} = \bar{A}(\bar{B} + \bar{C})$$

other relations:

Prove $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$

$(A+B)(\bar{A}+C)(B+C) = (0 + AC + \bar{A}B + BC)(B+C) = ABC + AC + \bar{A}B + \bar{A}BC + BC$

$= AC + \bar{A}B + BC = AC + \bar{A}B + BC + A\bar{A} = A(\bar{A}+C) + B(\bar{A}+C) = (A+B)(\bar{A}+C)$

Ex. Simplify $AB + A\bar{B}\bar{C} + \bar{A}BC$

$AB + A\bar{B}\bar{C} + \bar{A}BC = ABC + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC = BC + A\bar{C}$

Ex. Simplify $\bar{B}\bar{C}\bar{D} + B\bar{C}\bar{D} + A\bar{C}D$

$\bar{B}\bar{C}\bar{D} + B\bar{C}\bar{D} + A\bar{C}D = \bar{C}\bar{D} + A\bar{C}D = \bar{A}\bar{C}\bar{D} + A\bar{C}\bar{D} + A\bar{C}D = A\bar{C} + \bar{C}\bar{D}$

Note that $A\bar{C}\bar{D}$ is used twice which is ok in boolean algebra because $A + A = A \Rightarrow A\bar{C}\bar{D} + A\bar{C}\bar{D} = A\bar{C}\bar{D}$.

Ex. Simplify $A + B + C + \overline{ABC}$.

$A + B + C + \overline{ABC} = A + B + C + \bar{A} + \bar{B} + \bar{C} = 1 + 1 + 1 = 1$

Truth table.

Boolean Functions are Functions of boolean variables.

$$F = A + \bar{B}\bar{C}$$

Here, A, B and C can only take values of 0 or 1. F is a boolean function of these three variables and can only take values of 0 and 1. We can always draw a table of all possible combinations of values that A, B and C can take and find the values of F corresponding to these combinations. This table is called a truth table. Let's draw the truth table for function F.

| A | B | C | $\bar{B}$ | $\bar{C}$ | $\bar{B}\bar{C}$ | $F = A + \bar{B}\bar{C}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Note that F is taking only values of 0 and 1.

You can always prove an equality like the examples we did before by drawing a truth table that computes the two sides of the equality to make sure they are the same

ex. look at the proof of $\overline{A+B} = \bar{A} \cdot \bar{B}$

EX. Draw the truth table for the function L defined on page 4

There are three people involved in this problem: A, B and C. If any of them wants to give a launch-ready condition of True, its variable will be 1. If any of them wants to give a launch-ready condition of False, its variable will be 0.

| A | B | C | L |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

L is the final decision on whether launch-ready condition is true or false.

If C is 1 and either A or B is 1, then L is 1.

Minterms and maxterms:

Any boolean Function can be written in terms of simpler Functions called minterms or maxterms. To write a Function in terms of its minterms or maxterms, we First draw the truth table For the Function. suppose the truth table For a Function F of Two variables is given by

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

minterms involve the <u>and</u> operation. For every combination of values of A and B, we <u>and</u> A, B or their complements in such a way that the result is 1 (true).

| A | B | minterms of A and B |
|---|---|---|
| 0 | 0 | $m_0 = \bar{A}\,\bar{B}$ note that if $A=0, B=0$ Then $m_0 = 1$ |
| 0 | 1 | $m_1 = \bar{A}\,B$ " " " $A=0, B=1$ " $m_1 = 1$ |
| 1 | 0 | $m_2 = A\,\bar{B}$ " " " $A=1, B=0$ " $m_2 = 1$ |
| 1 | 1 | $m_3 = AB$ " " " $A=1, B=1$ " $m_3 = 1$ |

To write F in terms of its minterms, we just <u>or</u> those minterms For which the Function is 1 (true).

$$F = \bar{A}\,\bar{B} + AB$$

Draw the truth table For this boolean Function and see that You get the truth table we started with.

This Form of The Function is called the Sum of Product (SOP).

Maxterms involve the or operation. For every combination of values of A and B, we or A, B or their complements in such a way that the result is 0 (False).

| A | B | maxterms of A and B | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | $M_0 = A + B$ | note that | if | $A=0, B=0$ | then | $M_0 = 0$ |
| 0 | 1 | $M_1 = A + \bar{B}$ | " | " | $A=0, B=1$ | " | $M_1 = 0$ |
| 1 | 0 | $M_2 = \bar{A} + B$ | " | " | $A=1, B=0$ | " | $M_2 = 0$ |
| 1 | 1 | $M_3 = \bar{A} + \bar{B}$ | " | " | $A=1, B=1$ | " | $M_3 = 0$ |

To write F in terms of its maxterms, we just and those maxterms for which the Function is 0 (False).

$$F = (A + \bar{B})(\bar{A} + B)$$

Draw the truth table for this boolean Function and see that you get the truth table we started with.

This Form of the Function is called the Product of Sum (POS)

$$F = \bar{A}\bar{B} + AB = (A + \bar{B})(\bar{A} + B)$$

You can use boolean algebra to show these two expressions are equal.

Note: Two boolean variables A and B have four minterms and four maxterms. Not all of these minterms or maxterms contribute to F. For SOP, only those minterms for which $F=1$. For POS, only those maxterms for which $F=0$.

Three-variable minterms and maxterms:

| A | B | C | minterms | maxterms |
|---|---|---|---|---|
| 0 | 0 | 0 | $m_0 = \bar{A}\bar{B}\bar{C}$ | $M_0 = A+B+C$ |
| 0 | 0 | 1 | $m_1 = \bar{A}\bar{B}C$ | $M_1 = A+B+\bar{C}$ |
| 0 | 1 | 0 | $m_2 = \bar{A}B\bar{C}$ | $M_2 = A+\bar{B}+C$ |
| 0 | 1 | 1 | $m_3 = \bar{A}BC$ | $M_3 = A+\bar{B}+\bar{C}$ |
| 1 | 0 | 0 | $m_4 = A\bar{B}\bar{C}$ | $M_4 = \bar{A}+B+C$ |
| 1 | 0 | 1 | $m_5 = A\bar{B}C$ | $M_5 = \bar{A}+B+\bar{C}$ |
| 1 | 1 | 0 | $m_6 = AB\bar{C}$ | $M_6 = \bar{A}+\bar{B}+C$ |
| 1 | 1 | 1 | $m_7 = ABC$ | $M_7 = \bar{A}+\bar{B}+\bar{C}$ |

Ex. write the Function defined by the truth table below in terms of minterms (SOP) and maxterms (POS).

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

SOP

$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$

$= \bar{A}\bar{B} + A\bar{B} = \bar{B}$

POS

$F = (A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})$

$= (A+\bar{B})(\bar{A}+\bar{B}) = A\bar{B} + \bar{A}\bar{B} + \bar{B} = \bar{B}$

Forming a truth table From a boolean expression:

In this handout, we started From a truth table and obtained its boolean expression in SOP and POS Forms. The opposit. can also happen. we can start with a boolean expression and obtain its truth table.

Ex. let $F = \bar{A}BC + A\bar{B}C + ABC + AB\bar{C}$

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |

just substitute the values of A, B and C in every row and Find the value For F.

let $F = (\bar{A} + B)C$

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

# ENGR. 364
## Handout #27

Everything we have done so far in a nutshell:

1) we defined boolean variables such as $A, B, C$. These variables can only take values of 0 or 1.

2) we defined three basic operations AND ($\cdot$), OR ($+$) and not ($-$).

3) Combining boolean variables and these basic operation, we can define boolean functions such as $F = A \cdot \bar{B} + \bar{C} \cdot D$

4) we simplified boolean functions using boolean algebra.

$$F = A + B + \bar{A}B = A + B \cdot 1 + \bar{A}B = A + B(1 + \bar{A}) = A + B$$

5) Note that boolean functions can only take values of 0 and 1 only just like boolean variables.

6) other than specifying a boolean function in terms of a boolean expression, we can also specify it in terms of a truth table.

$F = A + \bar{B}$

| A | B | $\bar{B}$ | $F = A + \bar{B}$ |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |

7) If a function is specified in terms of a truth table, we can write it in terms of a boolean expression by using minterms (SOP) or maxterms (POS). we can then simplify these expressions using boolean algebra.

8) If a function is specified in terms of a truth table, we can simplify it using a technique called karnaugh map. This approach is easier than doing boolean algebra. Note that if we want to simplify a function specified by a boolean expression, we can first write it as a truth table and then use K-map.

Karnaugh map:

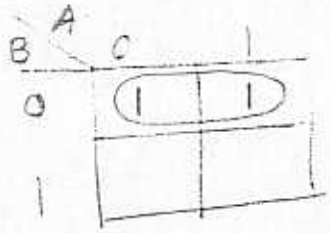
When you simplify boolean functions using boolean algebra, you can never be sure the simplest form is found. Karnaugh map is a technique for obtaining the simplest form of a boolean function

1) Consider a function of two variables.

Ex. $F = A\overline{B} + \overline{A}\,\overline{B}$

We know that $F = \overline{B}$ from boolean algebra.

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

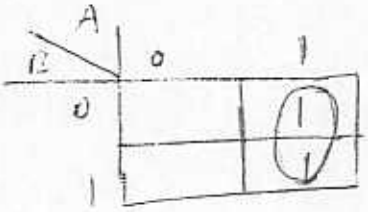



$F = \bar{B}$

When we combine the two cells only write down the variable(S) that does not change

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

$F = A\bar{B} + AB = A$




$F = A$

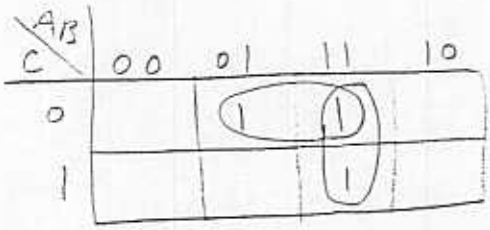
IF a variable stays at a value of zero in moving from one cell to another, we complement it. IF it stays at a value of 1, we do not complement.

2, Consider Functions of three variables:

| A | B | C | |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$F = \bar{A}B\bar{C} + AB\bar{C} + ABC$

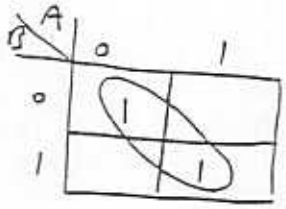
$= B\bar{C} + AB$




$F = B\bar{C} + AB$

Note that the $ABC = 110$ term is taken twice.

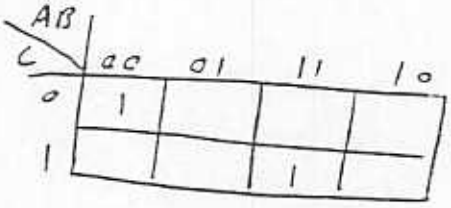
Karnaugh map (cont.):




In moving from one cell to the other, there is more than one variable changing value.

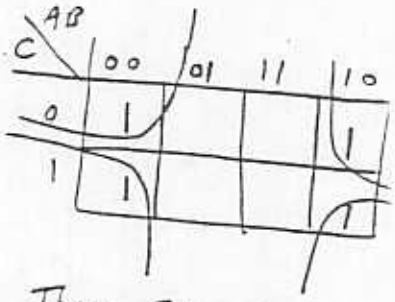
$F = \bar{A}\bar{B} + AB$ ← From the truth table for F

This expression can not be simplified anymore ⇒ When there is more than one variable changing in going from one cell to another, those two cells can not be combined in K. map.




Note: AB values are written such that only one variable changes when we go from one cell to the adjecent cell. Again, the two cells can not be combined because there is more than one variable changing.

$F = \bar{A}\bar{B}\bar{C} + AB\bar{C}$

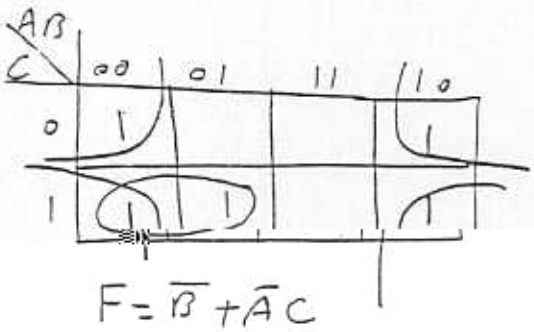



These four terms can be combined because we can go from one cell to another in such a way that only one variable changes.

$F = \bar{B}$

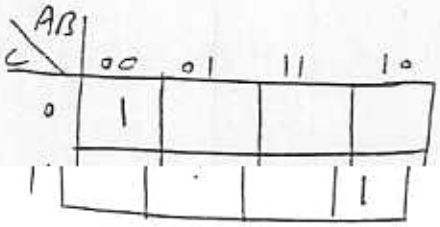
If we move to all cells, only B doesn't change. It stays at B=0

Ex.




$F = \bar{B} + \bar{A}C$

Ex.

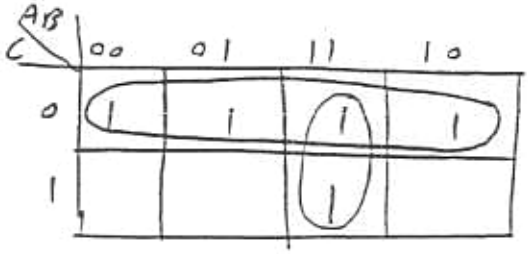



Can not be combined.

$F = \bar{A}\bar{B}\bar{C} + A\bar{B}C$

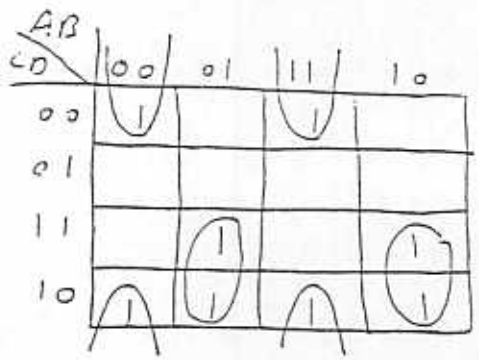
These are the two minterms that make up F from the truth table.

Ex.



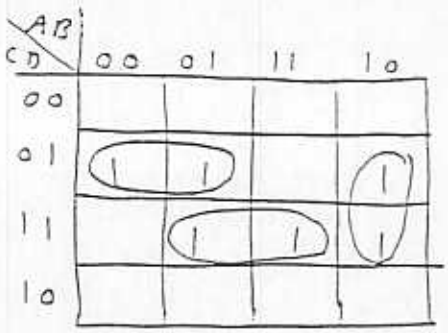

$F = \bar{C} + AB$

Ex.



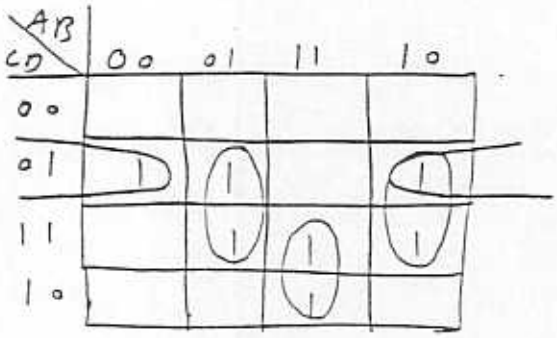

$F = \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}\bar{D} + AB\bar{D}$

Ex.

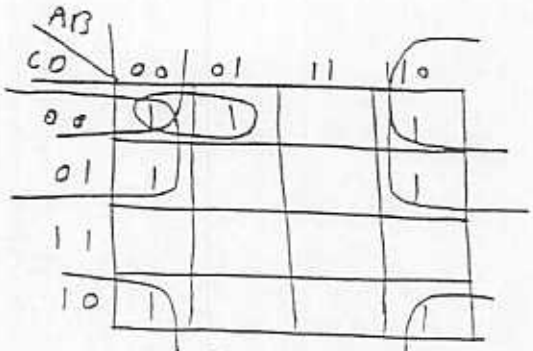



$F = \bar{A}\bar{C}D + BCD + A\bar{B}D$

Ex.

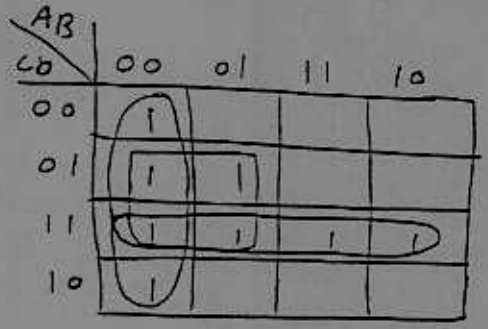



$F = \bar{A}B\bar{C}D + AB\bar{C} + A\bar{B}\bar{C}D + \bar{B}\bar{C}D$




$F = \bar{A}\bar{C}\bar{D} + \bar{B}\bar{D} + \bar{B}\bar{C}$

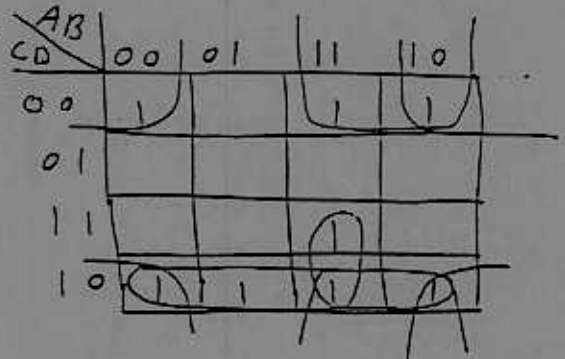
Ex.




$F = \bar{A}\bar{B} + CD + \bar{A}D$

Ex. Simplify $F = AB\bar{C}\bar{D} + C\bar{D} + ABCD + \bar{B}\bar{E}$

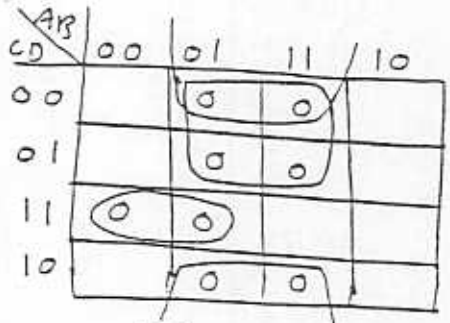
First, draw the truth table F. this Function and then transform that to K. map to get




$F = C\bar{D} + \bar{B}\bar{D} + ABC + A\bar{D}$

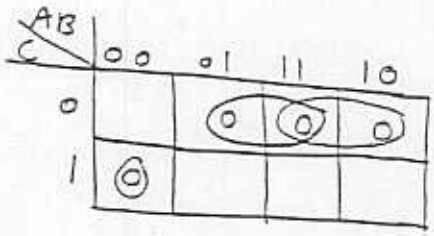
Up to now, we have used those values of the variable for which the function is 1 in the K map to find the simplified form of the function in SOP form. We can also use the combinati of values of variables for which the function is zero to obta a simplified form of F in POS form.

Ex




$F = (\bar{B}+C)(\bar{B}+D)(A+\bar{C}+\bar{D})$

Ex.



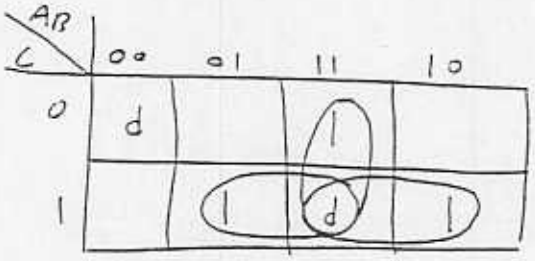

$F = (\bar{A}+C)(\bar{B}+C)(A+B+\bar{C})$

Ex. Find the boolean expression for a function of three variables which is true when two and only two of the variables are true. It is false only when one of the variables is true. It is either True or False (don't care) for any other combination of variables.

The truth table for this function is

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | d |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | d |

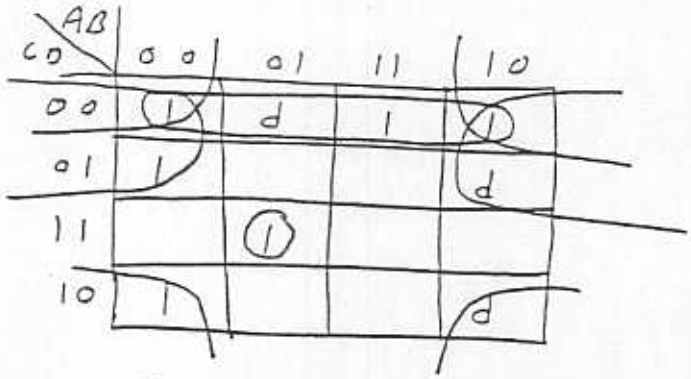
d stands for don't care.




$F = BC + AC + AB$

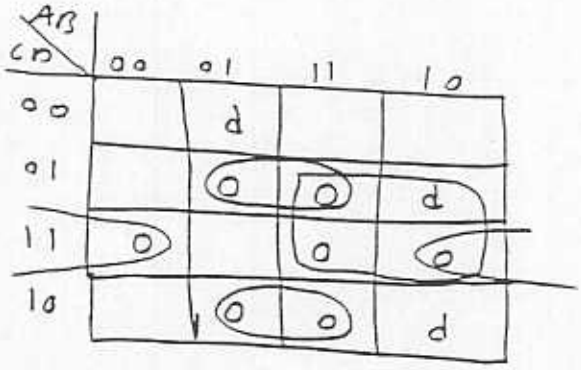
The value of a don't care can be 0 or 1. We include d in the K map and take its value to be 0 or 1 depending on which would give a more simplified F. In this problem, one d is used as 0 and one as 1.

Ex. For the K map shown below, Find the SOP and POS Form of F.




$F = \bar{C}\,\bar{D} + \bar{B}\,\bar{D} + \bar{B}\,\bar{C} + \bar{A}BCD$

SOP Form




$F = (\bar{A} + \bar{D})(\bar{B} + \bar{C} + D)(\bar{B} + C + \bar{D})(B + \bar{C} + \bar{D})$

POS Form

Truth table:

| A | B | C | D | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | d |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | d |
| 1 | 0 | 1 | 0 | d |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Notes:

1) First, we Find all the cells where the Function is 0. These are all the empty cells in the K map shown on the left.

2) We carry don't care to the new map since they can be either 0 or 1.

3) Some of the don't cares used on the left are not used on the right $\Rightarrow$ the two SOP and POS Forms do not have to be equal. They are only equal where the Function is definitely 1 or 0.

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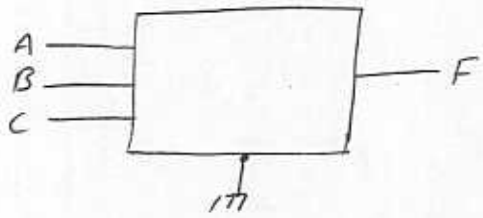
Handout #29

## Gates:

A gate is a many-input, one-output device. A gate is made of electrical components such as resistors, capacitors, diodes and transistors. A three-input, one-output device is shown as

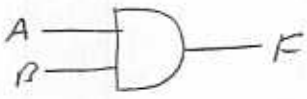



Here, A, B and C are input voltages and F is the output voltage. All input and output voltages are measured with respect to ground.

Inputs A, B and C are either set to $5^V$ or $0^V$. The output is then either $5^V$ or $0^V$. An input or output voltage of $5^V$ is assigned to a logic value of 1 (True). An input or output voltage of $0^V$ is assigned to a logic value of 0 (False).

## AND gate:

An AND gate perform the AND operation between two or more boolean variables.




$F = A \cdot B$

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Logic truth table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 5 | 0 |
| 5 | 0 | 0 |
| 5 | 5 | 5 |

Voltage truth table

The voltage truth table means, For example, if A and B are both set to 5V with respect to ground, F will be 5V with respect to ground.

## OR gate

An OR gate performs OR operation between two or more boolean variables.


$F = A + B$

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

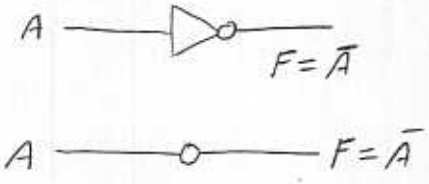
logic truth table

| A | B | F |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 5 | 5 |
| 5 | 0 | 5 |
| 5 | 5 | 5 |

Voltage truth table

## Not gate:

A NOT gate performs the Not operation



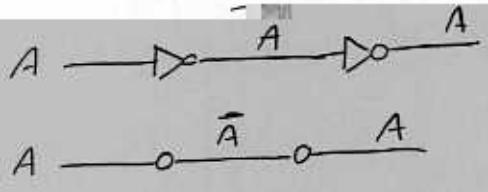

| A | F |
|---|---|
| 0 | 1 |
| 1 | 0 |

logic truth table

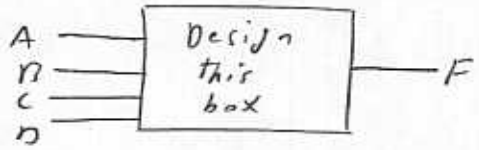
| A | F |
|---|---|
| 0 | 5 |
| 5 | 0 |

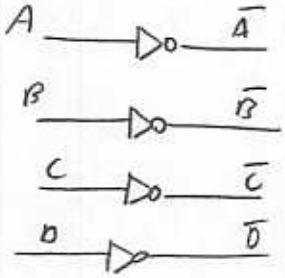
Voltage truth table

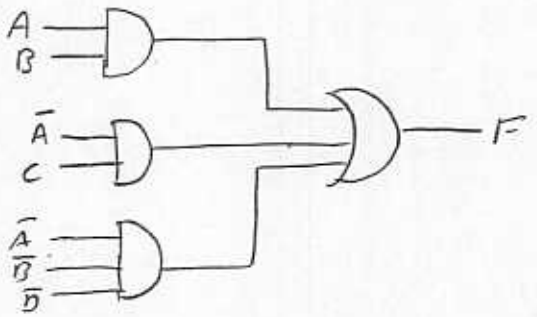
Note



Ex. Implement $F = AB + \bar{A}C + \bar{A}\bar{B}\bar{D}$ using logic gates.

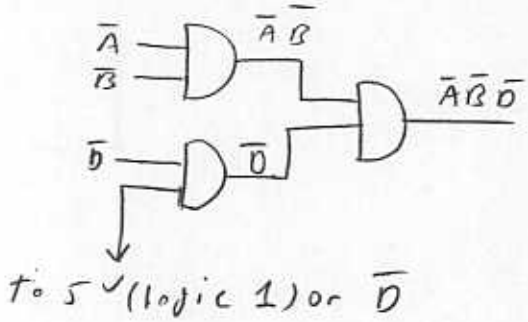



we need eight gates to implement F.

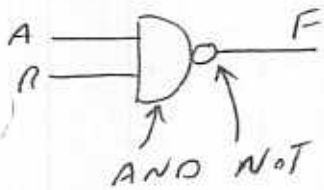
what if we do not have a three-input AND gate to implement $\bar{A}\bar{B}\bar{D}$.




other available gates:

NAND gate:

A NAND operation is an AND operation followed by a not operation.

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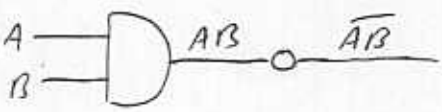


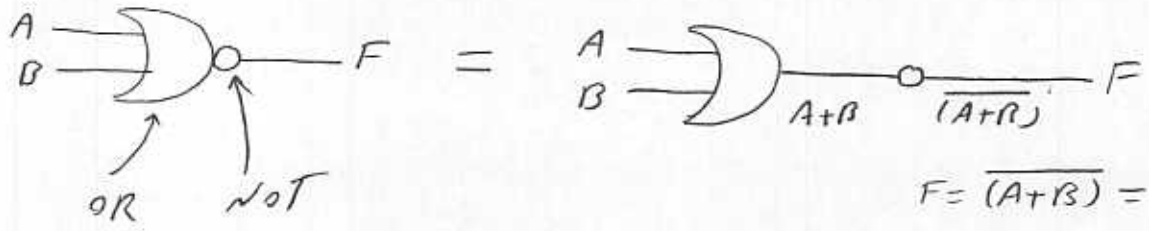

$F = \overline{(AB)} = \bar{A} + \bar{B}$

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

logic truth table

NOR gate:

A NOR operation is an OR operation followed by a NOT operation.

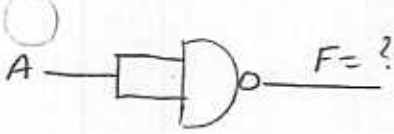



$F = \overline{(A+B)} = \bar{A}\,\bar{B}$

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

logic truth table

Some important observations:



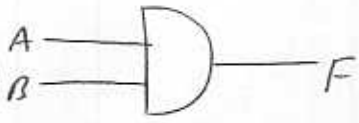

$F = \overline{(A \cdot A)} = \bar{A}$

If the two inputs of a NAND gate are tied together, it implements a NOT operation.


$F = \bar{A}B$

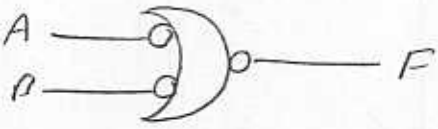
$F = \overline{(A+\bar{B})} = \bar{A}B$

You can always change an AND gate to an OR gate by putting bubbles (NOT operation) where inputs and output do not have them and taking them out of where they exist.

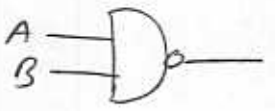



$F = AB$

=




$F = \overline{(\bar{A} + \bar{B})} = AB$

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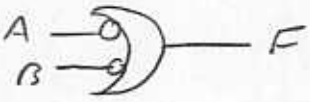
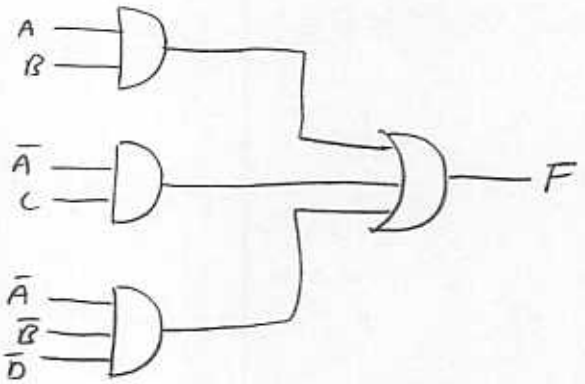
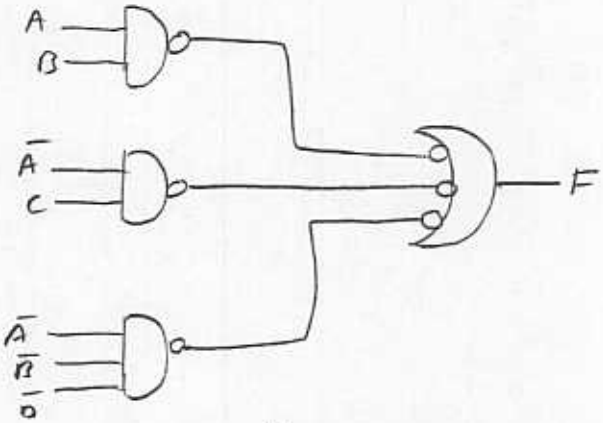


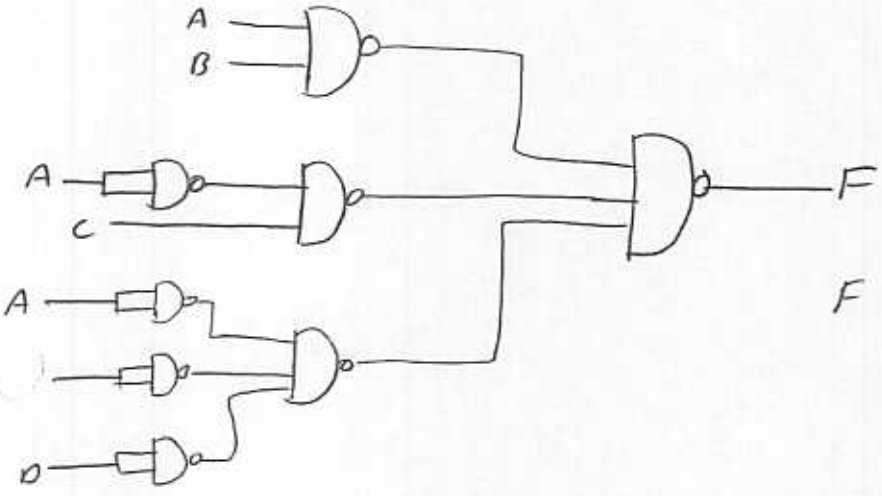

Ex. Implement $F = AB + \bar{A}C + \bar{A}\bar{B}\bar{D}$ using NAND gates only.




⇒



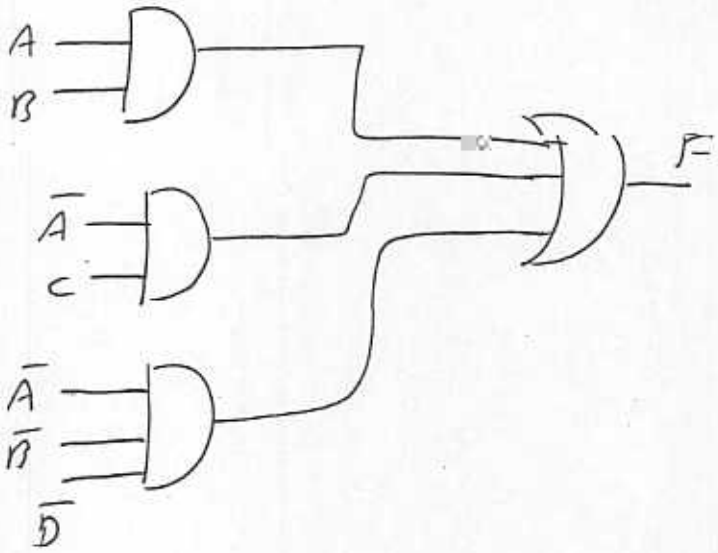

two bubbles is the same as no bubble.

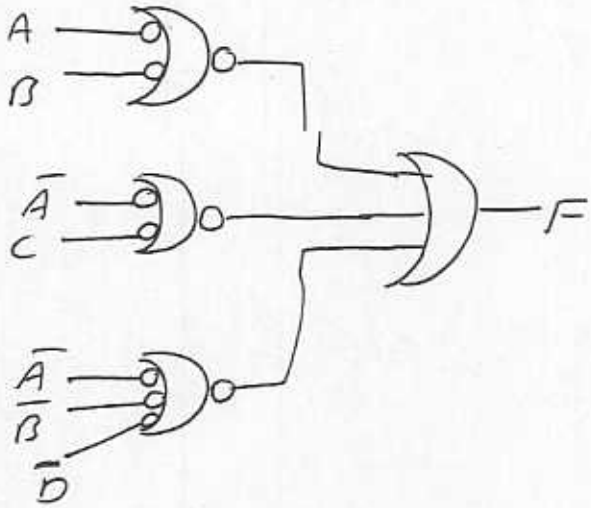


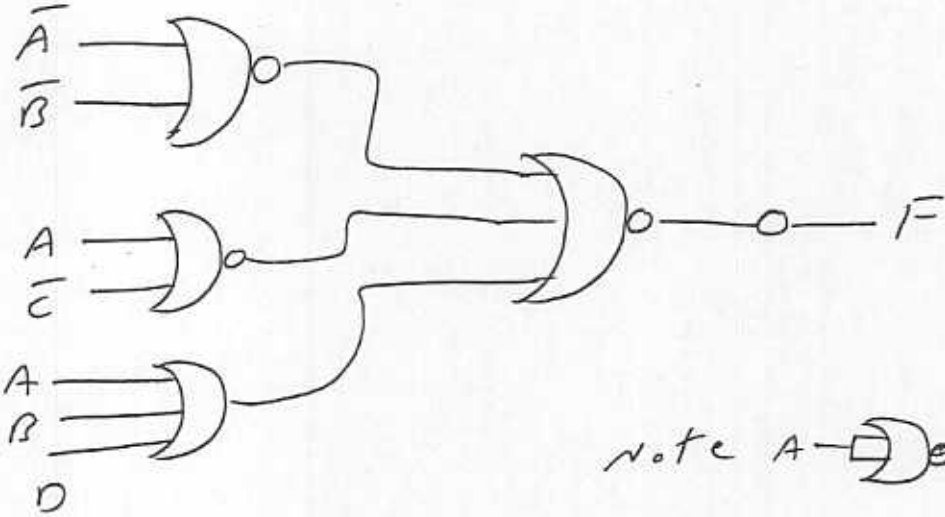

✓

F requires eight NAND gates.

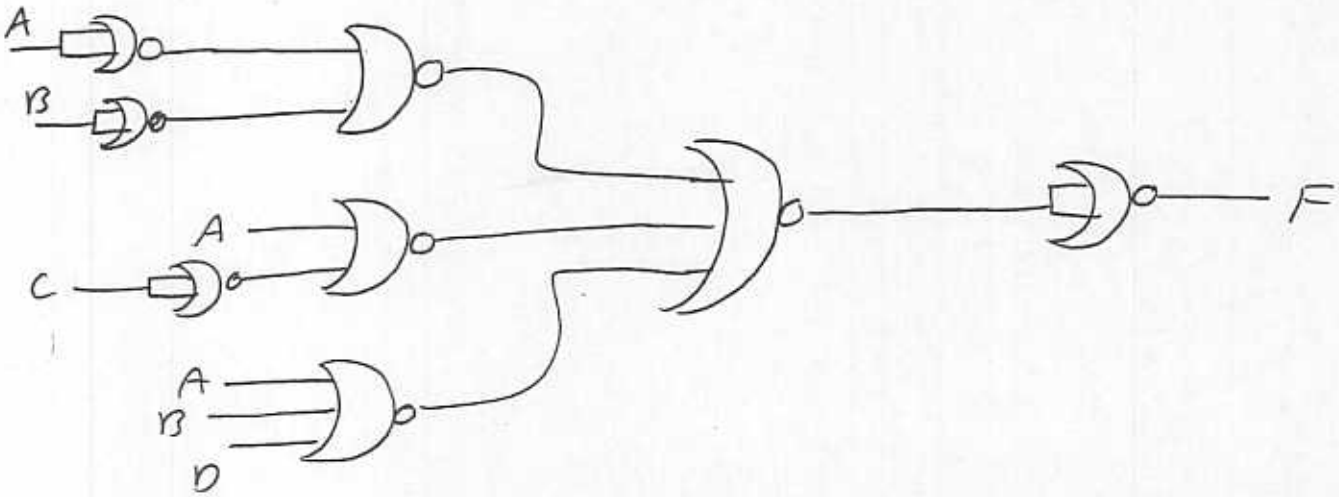
Ex. Implement $F = AB + \bar{A}C + \bar{A}\bar{B}\bar{D}$ using NOR gates only.



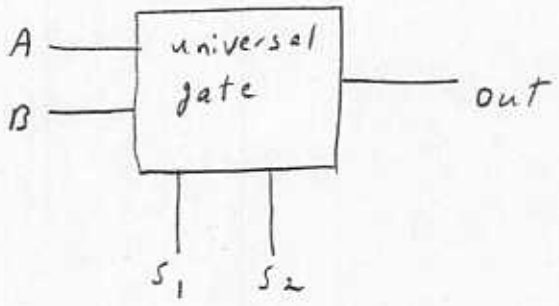

Note $A$ — $\overline{(A+A)} = \bar{A}$



Design Problems:

1) Design of a universal gate:

The purpose of this problem is to design a universal gate whose output (out) is the result of a logic operation (AND, OR, NAND, NOR) performed on A and B. The logic operation performed depends on the select lines $S_1$ and $S_2$ as shown below.



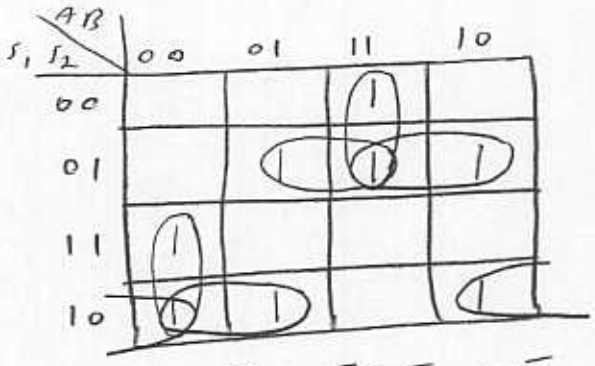

| $S_1$ | $S_2$ | out | |
|---|---|---|---|
| 0 | 0 | $A \cdot B$ | AND operation |
| 0 | 1 | $A + B$ | OR operation |
| 1 | 0 | $\overline{A \cdot B}$ | NAND operation |
| 1 | 1 | $\overline{A + B}$ | NOR operation |

This defines a universal logic gate that can perform any one of four logic operations depending on the selection lines.

In this problem, we design the universal gate.

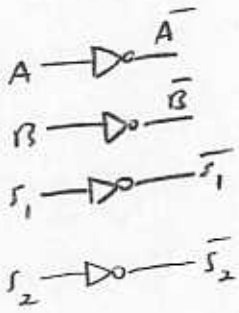
A, B, $S_1$, and $S_2$ are the four inputs to the gate.

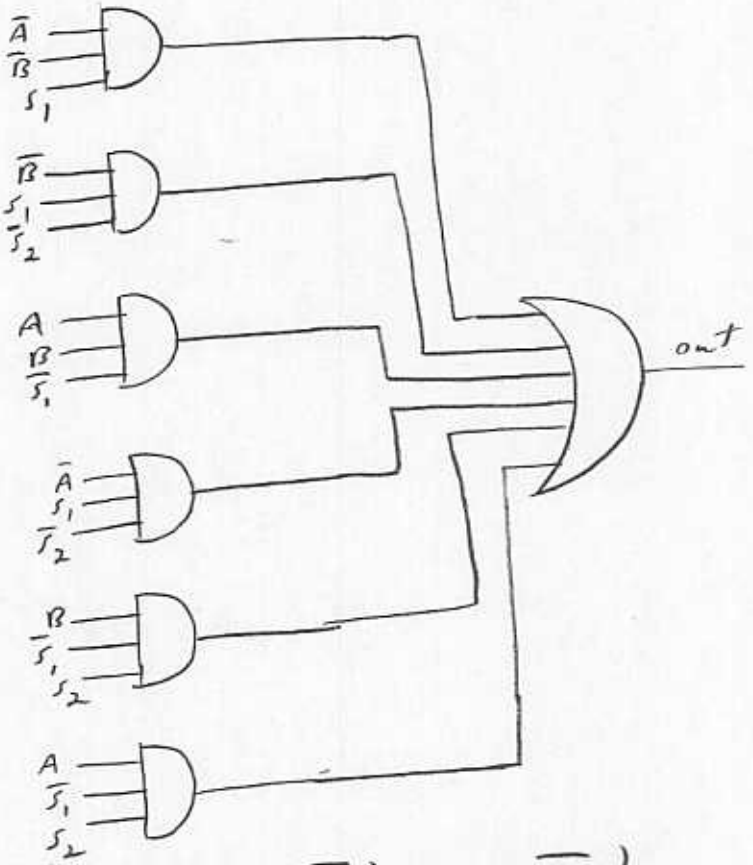
| A | B | $S_1$ | $S_2$ | out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $A \cdot B = 0$ |
| 0 | 0 | 0 | 1 | $A+B = 0$ |
| 0 | 0 | 1 | 0 | $\overline{A \cdot B} = 1$ |
| 0 | 0 | 1 | 1 | $\overline{A+B} = 1$ |
| 0 | 1 | 0 | 0 | $A \cdot B = 0$ |
| 0 | 1 | 0 | 1 | $A+B = 1$ |
| 0 | 1 | 1 | 0 | $\overline{A \cdot B} = 1$ |
| 0 | 1 | 1 | 1 | $\overline{A+B} = 0$ |
| 1 | 0 | 0 | 0 | $A \cdot B = 0$ |
| 1 | 0 | 0 | 1 | $A+B = 1$ |
| 1 | 0 | 1 | 0 | $\overline{A \cdot B} = 1$ |
| 1 | 0 | 1 | 1 | $\overline{A+B} = 0$ |
| 1 | 1 | 0 | 0 | $A \cdot B = 1$ |
| 1 | 1 | 0 | 1 | $A+B = 1$ |
| 1 | 1 | 1 | 0 | $\overline{A \cdot B} = 0$ |
| 1 | 1 | 1 | 1 | $\overline{A+B} = 0$ |




$$out = \bar{A}\bar{B}S_1 + \bar{B}S_1\bar{S_2} + AB\bar{S_1} + \bar{A}S_1\bar{S_2} + B\bar{S_1}S_2 + A\bar{S_1}S_2$$

Now, you can implement out using logic gates.




we can write $out = \bar{S_1}\bar{S_2}AB + \bar{S_1}S_2(A+B) + S_1\bar{S_2}(\overline{A \cdot B}) + S_1S_2(\overline{A+B})$

$= \bar{S_1}\bar{S_2}AB + \bar{S_1}S_2(A+B) + S_1\bar{S_2}(\bar{A}+\bar{B}) + S_1S_2(\bar{A}\bar{B})$

by inspection without the k-map. If we simplify this last expression using boolean algebra, we will obtain the same out as k-map.

All binary numbers can be represented in the decimal Form.

$$\underbrace{(abcd)_2}_{\text{binary Form}} = \underbrace{d\times 2^0 + c\times 2^1 + b\times 2^2 + a\times 2^3}_{\text{decimal Form}}$$

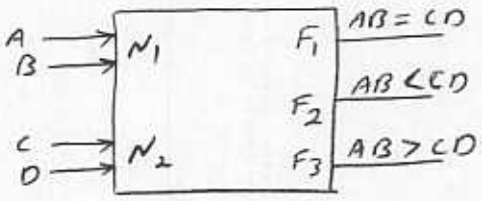
$$(1010)_2 = 0\times 2^0 + 1\times 2^1 + 0\times 2^2 + 1\times 2^3 = 0+2+0+8 = 10$$

| binary Form | decimal Form |
|---|---|
| 0 0 0 0 | 0 |
| 0 0 0 1 | 1 |
| 0 0 1 0 | 2 |
| 0 0 1 1 | 3 |
| 0 1 0 0 | 4 |
| 0 1 0 1 | 5 |
| 0 1 1 0 | 6 |
| 0 1 1 1 | 7 |
| 1 0 0 0 | 8 |
| 1 0 0 1 | 9 |
| 1 0 1 0 | 10 |
| 1 0 1 1 | 11 |
| 1 1 0 0 | 12 |
| 1 1 0 1 | 13 |
| 1 1 1 0 | 14 |
| 1 1 1 1 | 15 |

2) Two-bit comparator:

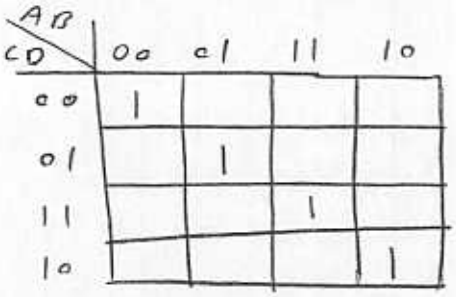
In this Problem, we design a circuit that takes as input two 2-bit numbers for comparison, $N_1$ and $N_2$. It generates three outputs $F_1$, $F_2$ and $F_3$ such that

$$\begin{cases} F_1 = 1 & \text{if } N_1 = N_2 \\ F_2 = 1 & \text{if } N_1 < N_2 \\ F_3 = 1 & \text{if } N_1 > N_2 \end{cases}$$

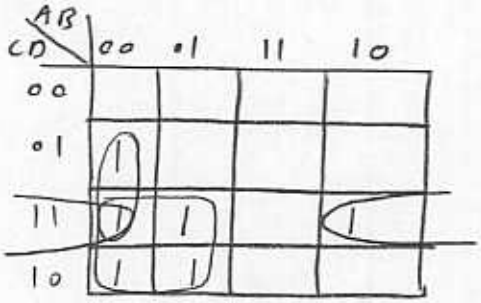



our goal is to design this circuit.

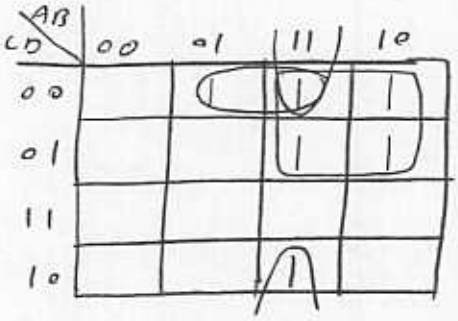
| A | B | C | D | $F_1$ | $F_2$ | $F_3$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |




$F_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D + A\bar{B}C\bar{D}$




$F_2 = \bar{A}C + \bar{A}\bar{B}D + \bar{B}CD$

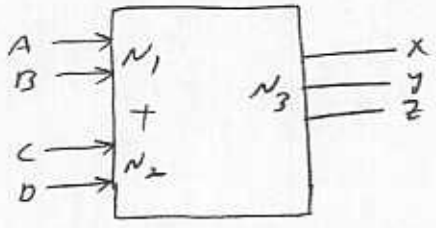



$F_3 = A\bar{C} + AB\bar{D} + B\bar{C}\bar{D}$

Now, we can implement $F_1$, $F_2$ and $F_3$ using logic gates.

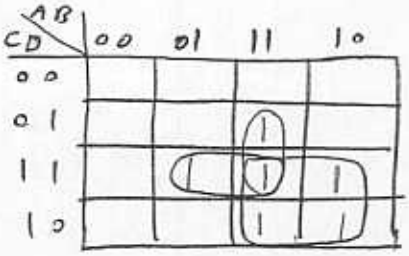
3) two-bit binary adder:

In this problem, we want to design a circuit that takes as input two 2-bit binary numbers $N_1$ and $N_2$. The output is a 3-bit binary number which is the sum of $N_1$ and $N_2$ in binary form.

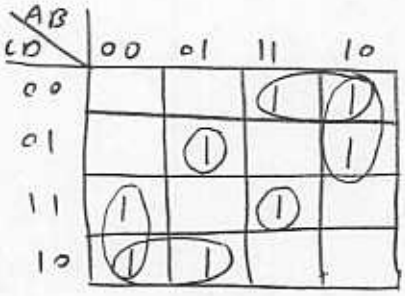



$N_3 = N_1 + N_2$

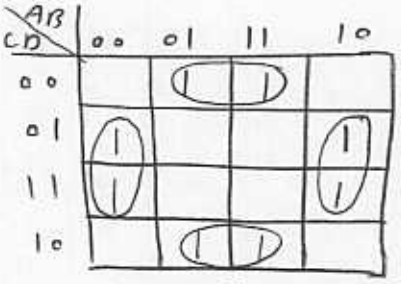
| A | B | C | D | | X | Y | Z |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0+0=0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0+1=1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0+2=2 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0+3=3 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1+0=1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1+1=2 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1+2=3 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1+3=4 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 2+0=2 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 2+1=3 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 2+2=4 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 2+3=5 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 3+0=3 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 3+1=4 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 3+2=5 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 3+3=6 | 1 | 1 | 0 |




$X = AC + \bar{B}CD + AB\bar{D}$




$Y = \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}C\bar{D} + A\bar{C}\bar{D} + \bar{A}B\bar{C}D + ABCD$

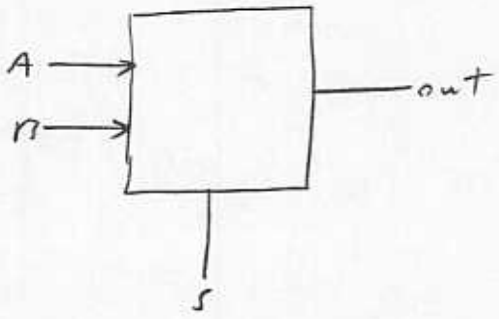



$Z = \bar{A}\bar{B}D + B\bar{C}\bar{D} + B\bar{C}\bar{D} + A\bar{B}D$

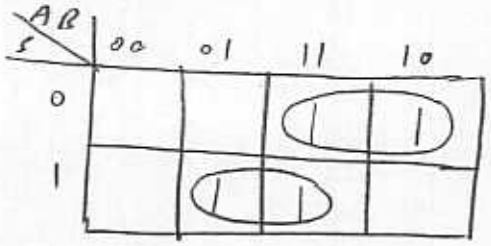
4) 2-input multiplexer:

In this problem, we design a 2-input multiplexer. This multiplexer has two inputs A and B and a selection line S also called address. Depending on the value of S, one of A or B is transmitted to the output.

$$out = \begin{cases} A & \text{if } S=0 \\ B & \text{if } S=1 \end{cases}$$



| A | B | S | out |
|---|---|---|---|
| 0 | 0 | 0 | 0 ← A |
| 0 | 0 | 1 | 0 ← B |
| 0 | 1 | 0 | 0 ← A |
| 0 | 1 | 1 | 1 ← B |
| 1 | 0 | 0 | 1 ← A |
| 1 | 0 | 1 | 0 ← B |
| 1 | 1 | 0 | 1 ← A |
| 1 | 1 | 1 | 1 ← B |



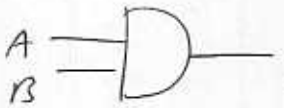

$out = A\bar{S} + BS$

You should be able to find the boolean expression for out without k-map (why?).

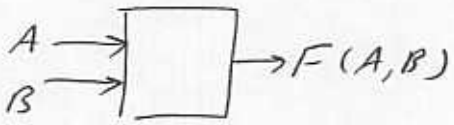
Handout #31

ENGR. 2364

So Far, we have considered combinational circuits such as AND, OR, NOT, NOR, and NAND gates. circuits made out of these gates are called combinational circuits since they produce an output which is only a Function of some inputs. For example, For an AND gate, we have




$F = A \cdot B$




Here, F is completely determined in terms of inputs A and B.

In contrast to combinational circuits, we have sequential circuits which are more complicated. In sequential machines, we have Flip-Flops which are electrical components with memory. These elements have what we call present state. Depending on the input given to them and their present state, they then go to what we call next state. The reason they have memory is because they remember their present state (they know where they are). The outputs in these machines is always a Function of inputs and present state.

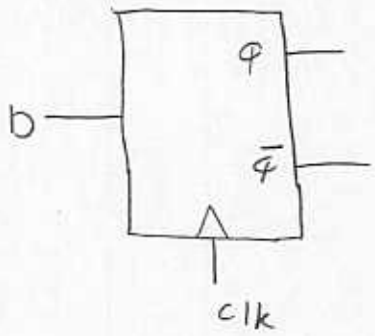
## Flip-Flops:

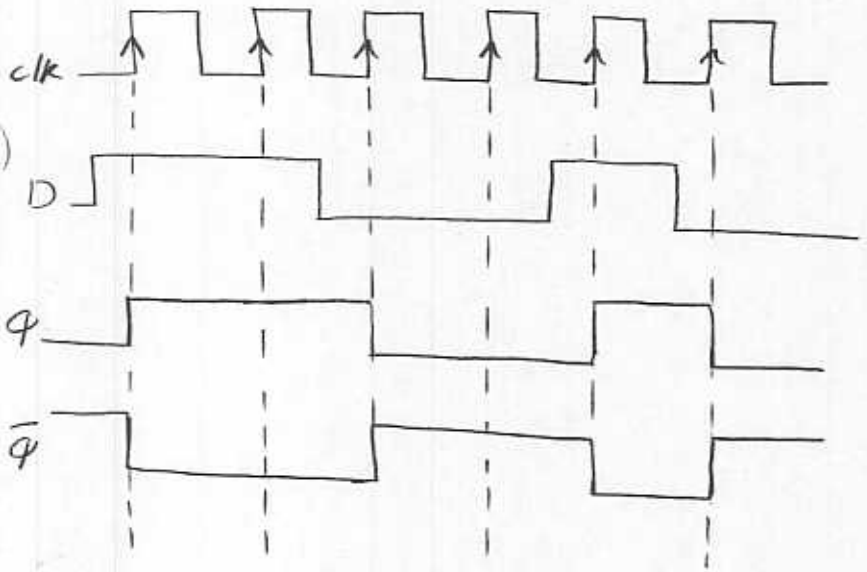
Flip-Flops are memory elements capable of storing input data.

### ① D (delayed) Flip-Flop:

A D Flip-Flop reads its input at the rising edge of the clock (clk) and sets $Q = D$ and $\bar{Q} = \bar{D}$.

Between the rising edges of the clk, Q is not allowed to change.

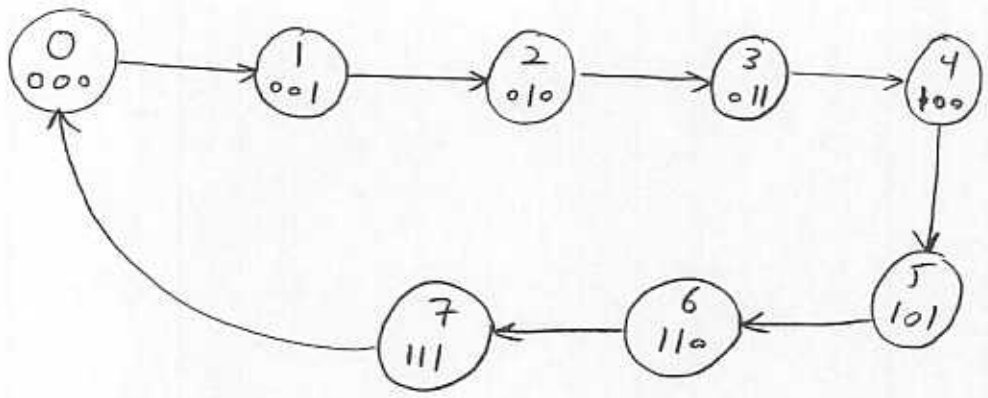



Sample D at the rising edge of the clk to set Q and $\bar{Q}$

A D Flip-Flop is a memory element because it samples the value of D at the rising edge of the clk and holds it in Q until the next rising edge of the clk.

A D Flip-Flop can be used to design a counter that counts From 0 to 7.



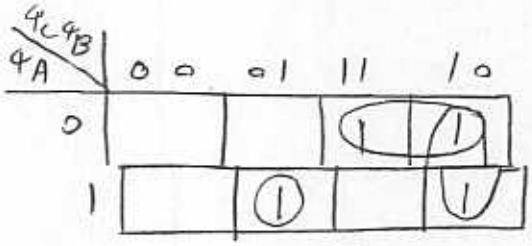

Count 0 1 2 3 4 5 6 7 0 1 2 3 . . . .

Let's design this counter using D Flip-Flops. We use 3 D Flip-Flops to represent the binary number equivalent to the decimal count of interest.

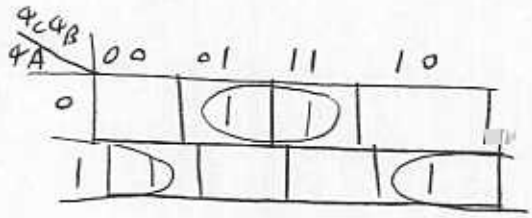
| Present count or Present state | | | Next Count or next state | | | Values of D required to make next state to happen | | |
|---|---|---|---|---|---|---|---|---|
| $Q_C$ | $Q_B$ | $Q_A$ | $Q_C$ | $Q_B$ | $Q_A$ | $D_C$ | $D_B$ | $D_A$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Notice That D values are equal to next state values because next state values represent where we want to be next which then determine the D values.

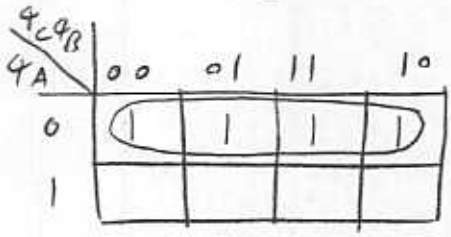
Now, we can draw a k-map For $D_C$, $D_B$ and $D_A$ in terms of The present states oF the machine $q_C q_B q_A$ which represent where the machine is right now.




$D_C = q_C \bar{q}_A + q_C \bar{q}_B + \bar{q}_C q_B q_A$




$D_B = q_B \bar{q}_A + \bar{q}_B q_A$




$D_A = \bar{q}_A$

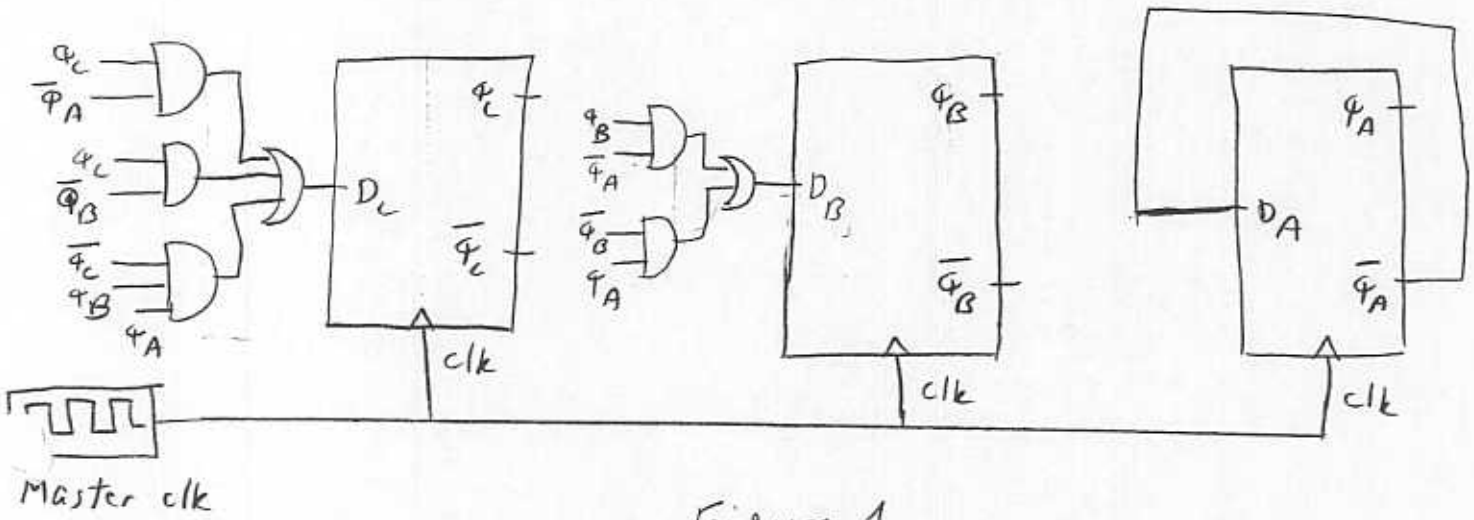
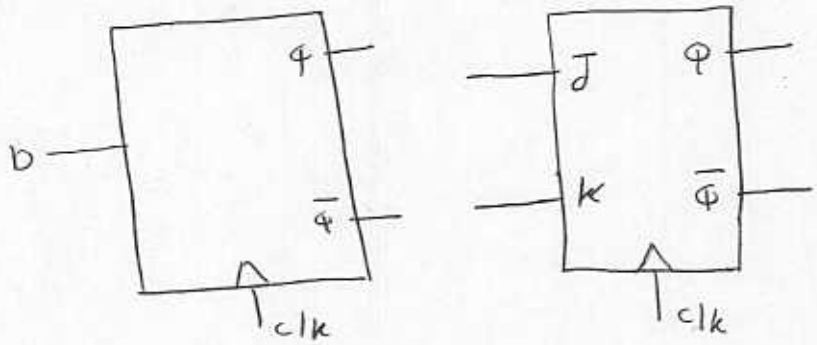



Figure 1

Note that the implementation of $D_C$, $D_B$ and $D_A$ involve $q_C$, $\bar{q}_C$, $q_B$, $q_A$ and $\bar{q}_A$. The wires connecting these $q$s and $\bar{q}$s to implement $D$s are not shown. These connections must be made for circuit to operate correctly.

## Jk Flip-Flop:

Jk Flip-Flops are another kind of memory elements similar to D Flip-Flops. As mentioned before, a D Flip-Flop acts as shown in table 1. At the rising edge of the clk shown




| D | clk | Q |
|---|---|---|
| 0 | ↑ | 0 |
| 1 | ↑ | 1 |

by ↑, D transfers to Q. Between the rising edges of the clk, Q can not change. The D Flip-Flop is only allowed to examine its input at the rising edge of the clk to adjust its output.

A Jk Flip-Flop is also controlled by the clk. At the rising edge of the clk(↑), the Jk Flip-Flop makes changes to Q. A Jk Flip-Flop is, however, more sophisticated than a D Flip-Flop as shown in table 2.

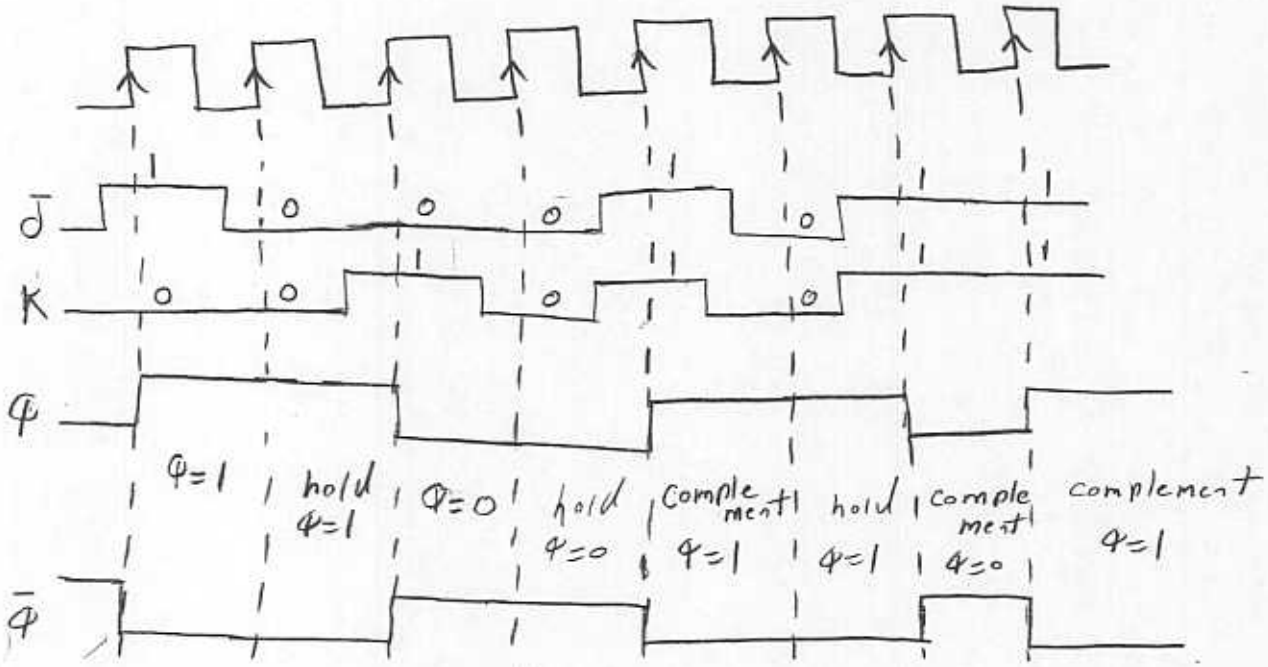
At the rising edge of the clk, a JK Flip-Flop examines its inputs J and K. IF J=k=0, then the Flip-Flop does not change its state. IF the present state is 0, the next state will be 0. IF the present state is 1, the next state is 1.

| J | K | clk | $Q^+$ |
|---|---|---|---|
| 0 | 0 | ↑ | $Q$ |
| 0 | 1 | ↑ | 0 |
| 1 | 0 | ↑ | 1 |
| 1 | 1 | ↑ | $\bar{Q}$ |

$Q$ = present state

$Q^+$ = next state

IF J=0 and k=1, the next state will always be 0. IF J=1, and K=0, the next state will always be 1. IF J=k=1, the next state will always be the complement of the present state. IF present state is 0, the next state will be 1. IF the present state is 1, the next state will be 0.




Assume $Q=0$ initially

Only at the rising edge of the clk, J, k and present value of $Q$ are evaluated to find the next state of the Flip-Flop.

Table 2 can be written in a different form called the excitation table of a JK Flip-Flop. We can consider a given present state and a desired next state and obtain the JK values that make this transition possible.

For example, let $Q=0$ and $Q^+=1$

To go from a present state of $Q=0$ to a next state of $Q^+=1$, we can either have

$$\begin{cases} J=1 \\ K=1 \end{cases} \quad \text{or} \quad \begin{cases} J=1 \\ K=0 \end{cases}.$$

Either way $Q=0$ results in the next state $Q^+=1$.

Therefore, we can write

| $Q$ | $Q^+$ | $J$ | $K$ |
|---|---|---|---|
| 0 | 1 | 1 | d |

similarly, we have

$Q=0,\ Q^+=0 \Rightarrow \begin{cases} J=0 \\ K=0 \end{cases}$ or $\begin{cases} J=0 \\ K=1 \end{cases} \Rightarrow \begin{cases} J=0 \\ K=d \end{cases}$

$Q=1,\ Q^+=0 \Rightarrow \begin{cases} J=1 \\ K=1 \end{cases}$ or $\begin{cases} J=0 \\ K=1 \end{cases} \Rightarrow \begin{cases} J=d \\ K=1 \end{cases}$

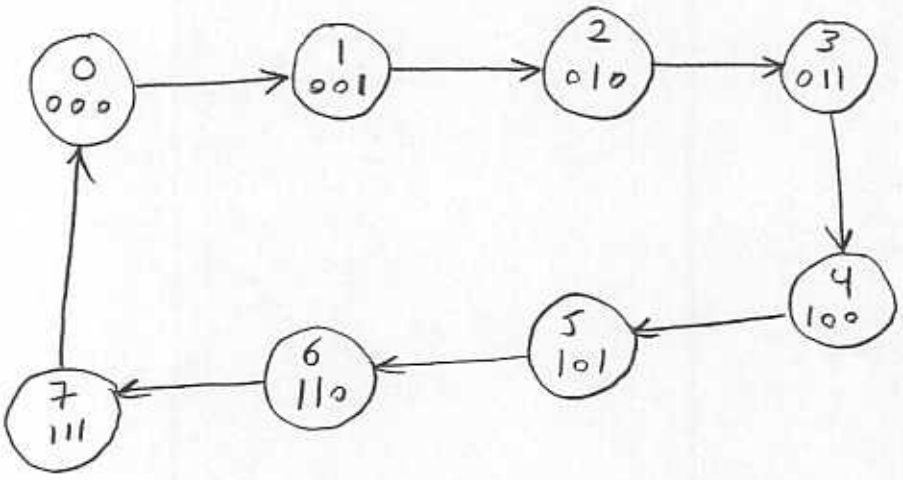
$Q=1,\ Q^+=1 \Rightarrow \begin{cases} J=0 \\ K=0 \end{cases}$ or $\begin{cases} J=1 \\ K=0 \end{cases} \Rightarrow \begin{cases} J=d \\ K=0 \end{cases}$

Excitation table

| $Q$ | $Q^+$ | $J$ | $K$ |
|---|---|---|---|
| 0 | 0 | 0 | d |
| 0 | 1 | 1 | d |
| 1 | 0 | d | 1 |
| 1 | 1 | d | 0 |

This table shows that to go from a present value of state $Q$ to next state $Q^+$ requires the JK values shown.

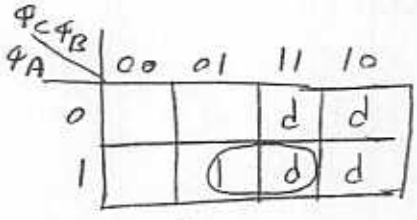
Ex. Design a counter that counts from 0 to 7 using Jk Flip-Flops.



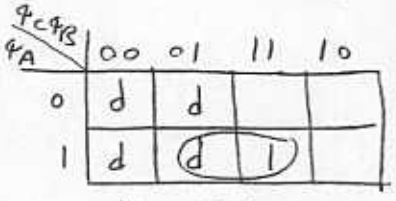

use 3 Jk Flip-Flops. The present state Q of each Flip-Flop will represent one of the binary numbers

| Present state | | | Next state | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $Q_C$ | $Q_B$ | $Q_A$ | $Q_C$ | $Q_B$ | $Q_A$ | $J_C$ | $K_C$ | $J_B$ | $K_B$ | $J_A$ | $K_A$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | d | 0 | d | 1 | d |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | d | 1 | d | d | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | d | d | 0 | 1 | d |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | d | d | 1 | d | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | d | 0 | 0 | d | 1 | d |
| 1 | 0 | 1 | 1 | 1 | 0 | d | 0 | 1 | d | d | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | d | 0 | d | 0 | 1 | d |
| 1 | 1 | 1 | 0 | 0 | 0 | d | 1 | d | 1 | d | 1 |

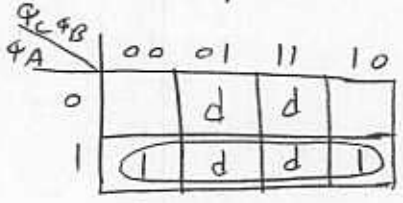
Next, draw k-maps For Js and ks in terms of present states.




$J_C = Q_B Q_A$




$K_C = Q_B Q_A$




$J_B = Q_A$

| $Q_A$ \ $Q_C Q_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | d | | | d |
| 1 | d | 1 | 1 | d |

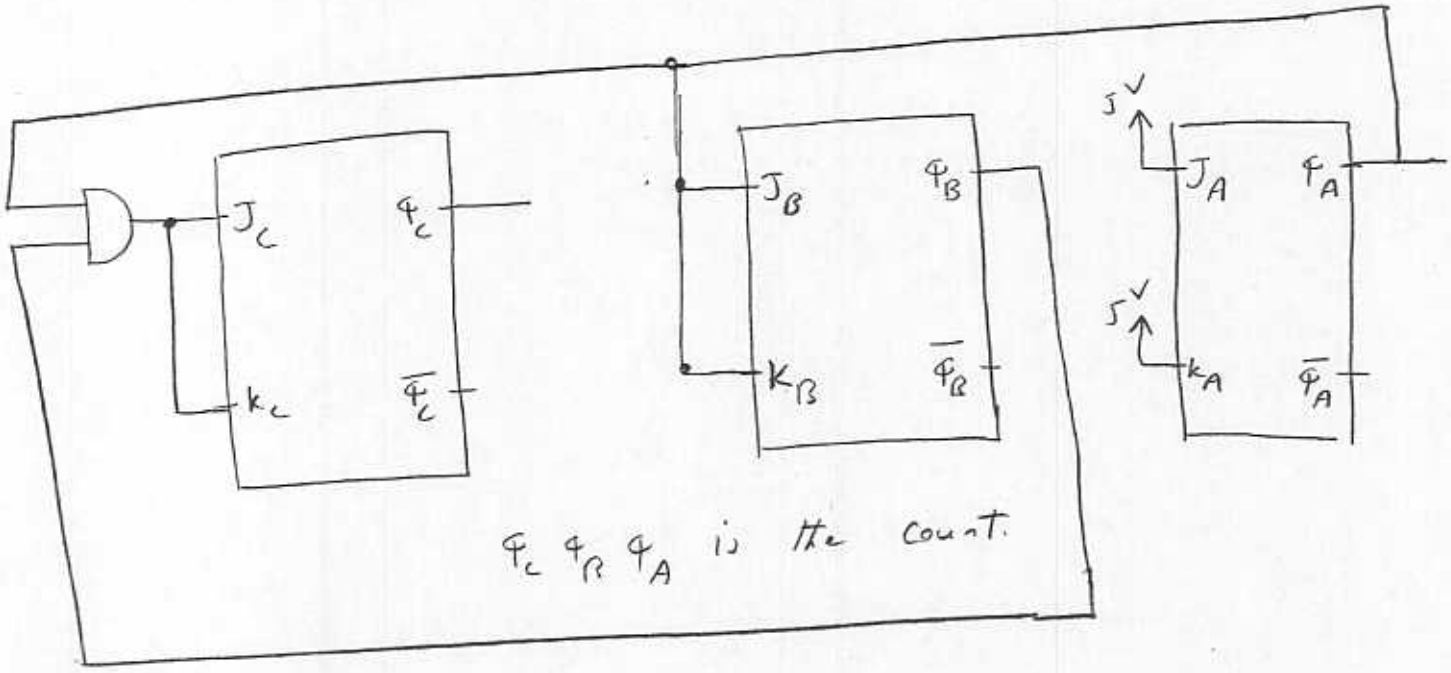
$K_B = Q_A$

| $Q_A$ \ $Q_C Q_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | d | 1 | 1 |
| 1 | d | d | d | d |

$J_A = 1$

| $Q_A$ \ $Q_C Q_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | d | d | d | d |
| 1 | 1 | 1 | 1 | 1 |

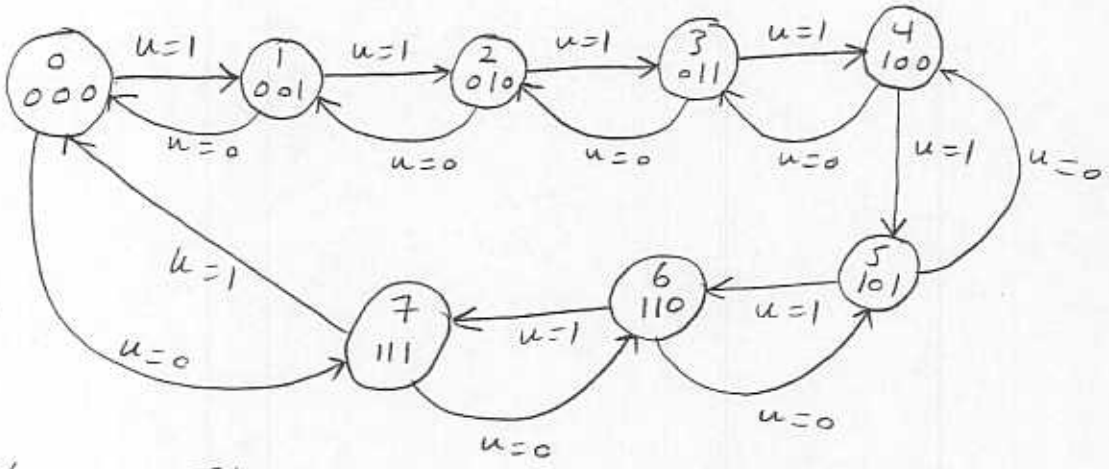
$K_A = 1$




All clks must be tied together and connected to master clk.

Handout #33

EX. Design a 3-bit up-down counter. This counter has an input $u$ that controls the count. IF $u=1$, count up. IF $u=0$, count down.



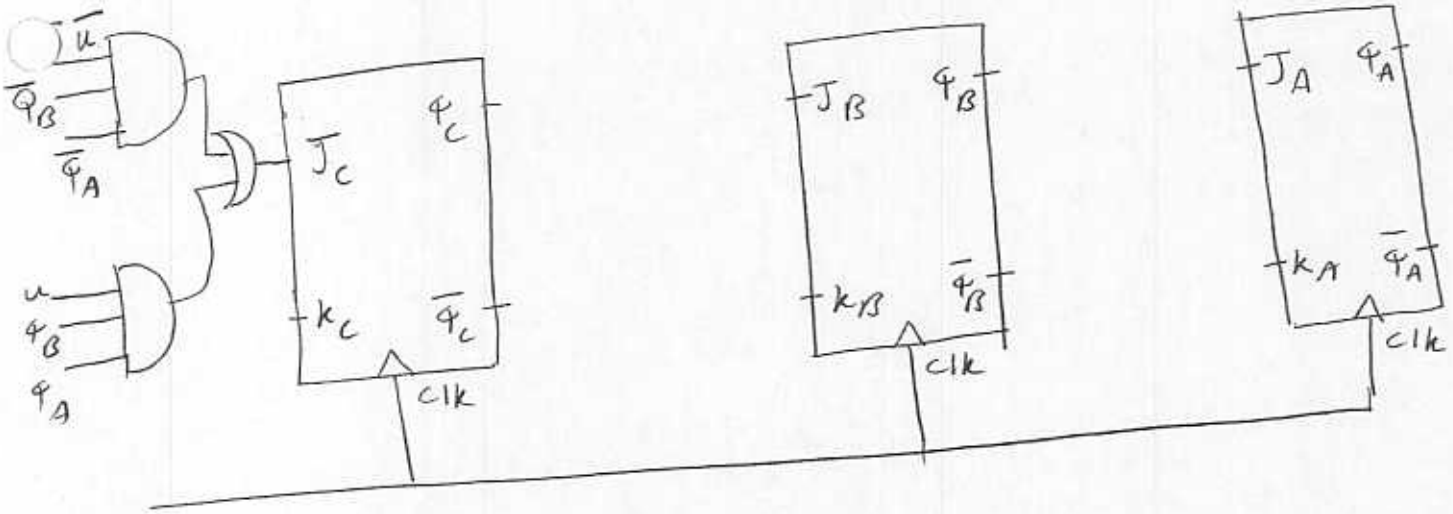

let's use JK Flip-Flops. We need three. The Flip-Flop states $Q_C Q_B Q_A$ will represent the count and $u$ controls the direction of the count.

| | input $u$ | present state $Q_C$ | $Q_B$ | $Q_A$ | Next state $Q_C$ | $Q_B$ | $Q_A$ | $J_C$ | $K_C$ | $J_B$ | $K_B$ | $J_A$ | $K_A$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Count down | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | d | 1 | d | 1 | d |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | d | 0 | d | d | 1 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | d | d | 1 | 1 | d |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | d | d | 0 | d | 1 |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | d | 1 | 1 | d | 1 | d |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0 | d | 0 | 0 | d | d | 1 |
| | 0 | 1 | 1 | 0 | 1 | 0 | 1 | d | 0 | d | 1 | 1 | d |
| | 0 | 1 | 1 | 1 | 1 | 1 | 0 | d | 0 | d | 0 | d | 1 |
| Count up | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | d | 0 | d | 1 | d |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | d | 1 | d | d | 1 |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | d | d | 0 | 1 | d |
| | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | d | d | 1 | d | 1 |
| | 1 | 1 | 0 | 0 | 1 | 0 | 1 | d | 0 | 0 | d | 1 | d |
| | 1 | 1 | 0 | 1 | 1 | 1 | 0 | d | 0 | 1 | d | d | 1 |
| | 1 | 1 | 1 | 0 | 1 | 1 | 1 | d | 0 | d | 0 | 1 | d |
| | 1 | 1 | 1 | 1 | 0 | 0 | 0 | d | 1 | d | 1 | d | 1 |

Next, draw k-maps to Find $J_s$ and $k_s$ in terms of u and present states of $q_C\ q_B\ q_A$, and draw the circuit diagram. For instance, let's do $J_C$.

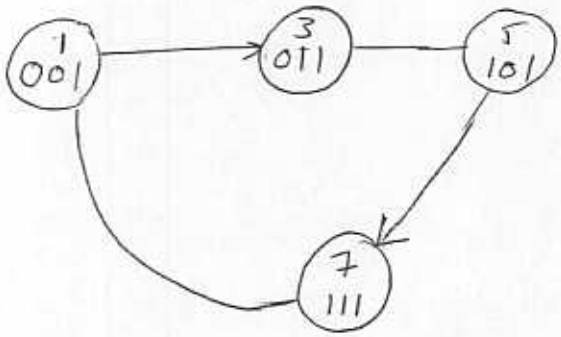
| $q_B q_A$ \ $u q_C$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | d | d | |
| 01 | | d | d | |
| 11 | | d | d | 1 |
| 10 | | d | d | |

$$k_C = \bar{u}\,\bar{q}_B\,\bar{q}_A + u\,q_B\,q_A$$




Finish the design by implementing $k_C$, $J_B$, $k_B$, $J_A$, $k_A$.

Ex. Design a counter that goes through the count shown.




We need 3 Flip-Flops to keep track of the count up to 7. Lets use D Flip-Flops.

| Present state | | | Next state | | | | | |
|---|---|---|---|---|---|---|---|---|
| $Q_C$ | $Q_B$ | $Q_A$ | $Q_C$ | $Q_B$ | $Q_A$ | $D_C$ | $D_B$ | $D_A$ |
| 0 | 0 | 0 | d | d | d | d | d | d |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | d | d | d | d | d | d |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | d | d | d | d | d | d |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | d | d | d | d | d | d |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

Note that out of states 0, 2, 4, 6 we go to don't care states because these states do not happen in the count and we don't care where we go from there. Now, we do k-maps for $D_C$, $D_B$, $D_A$ in terms of present states $Q_C$ $Q_B$ $Q_A$.

| $Q_C Q_B$ / $Q_A$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | d | (d) 1 | d | (d) 1 |
| 1 | | | | |

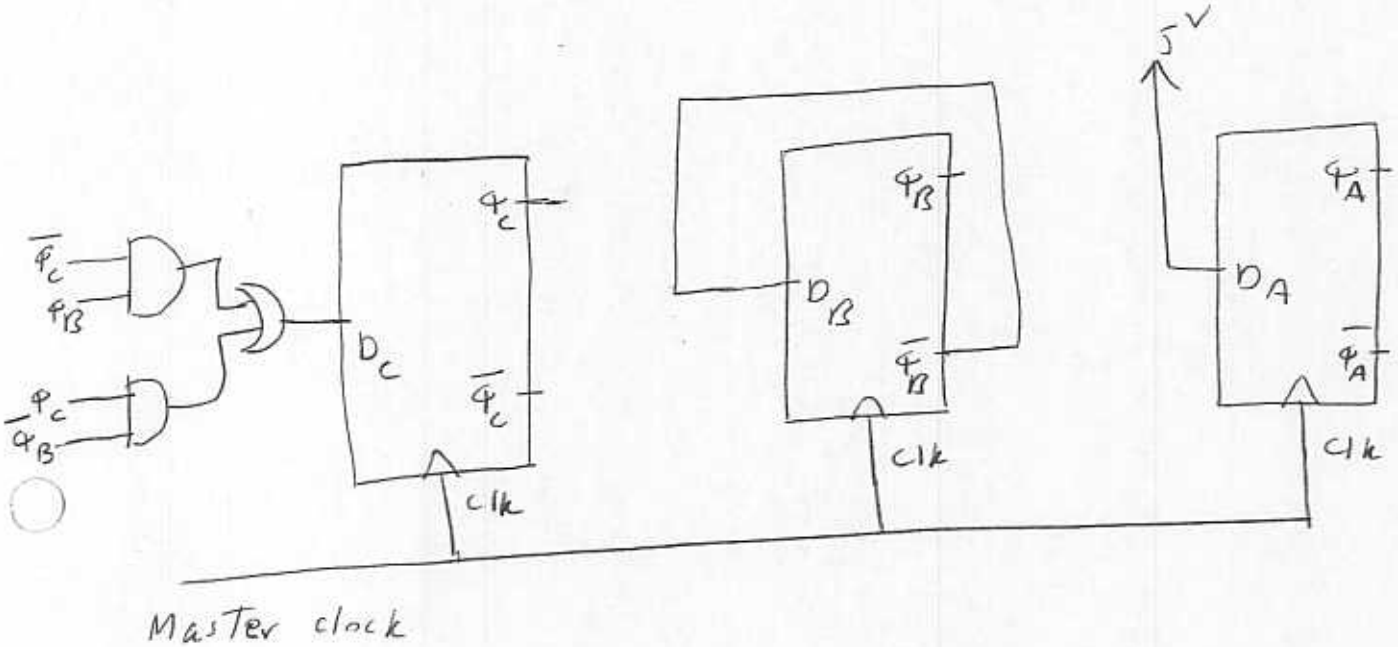
$D_C = \bar{Q}_C Q_B + Q_C \bar{Q}_B$

| $Q_C Q_B$ / $Q_A$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | (d) 1 | d | d | (d) |
| 1 | (1) | | | 1 |

$D_B = \bar{Q}_B$

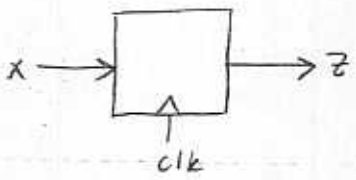
| $Q_C Q_B$ / $Q_A$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | d | d | d | d |
| 1 | 1 | 1 | 1 | 1 |

$D_A = 1$




Master clock

ex. Design a sequential machine that recognizes the sequence 010 by asserting its output.




input X: 0 0 1 0 1 0 1 0 0 1 0

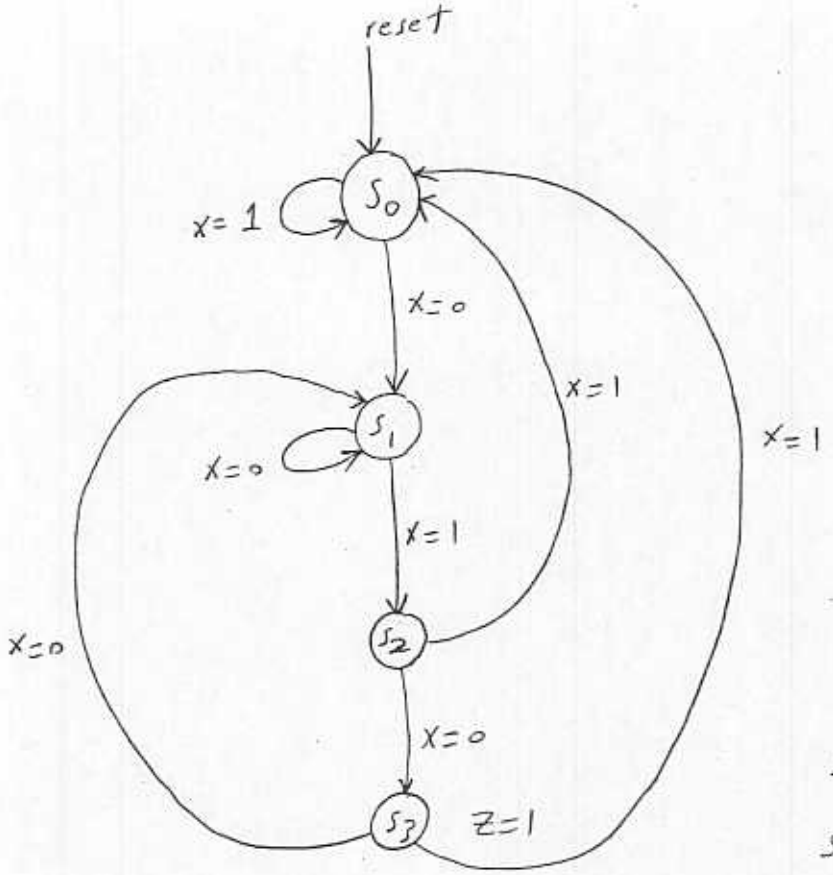
X: 0 0 1 0 1 0 1 0 0 1 0
Z: 0 0 0 1 0 1 0 1 0 0 1 ①

X: 1 1 0 1 1 0 1 0 0 1 0
Z: 0 0 0 0 0 0 0 1 0 0 1 ②

① & ② are two different ways you may want to design your machine. In ①, the last 0 in 010 can be the start of a new sequence. In ②, you are not allowing for this to happen. When you design your machine, you can accomodate ① or ② whichever you like.

Solution: Let's start with our sequential machine being in state $S_0$ which is the start up state. No digit from the sequence 010 is detected yet. This is the state you want to be in if 1) you want to start fresh and feed inputs x, 2) you start the sequential machine by turning the power on and 3) you walk to the machine not knowing what others have been feeding it as input. For the reasons given above, it is always a good idea to have another input to the machine called RESET such that when it is asserted (RESET = logic 1 or 5V), it takes the machine to $S_0$ no matter where the machine

had been.




| | |
|---|---|
| $S_0$ | — |
| $S_1$ | 0 |
| $S_2$ | 01 |
| $S_3$ | 010 |

At $S_0$, we have not started the sequence yet or the right first digit (0) has not come yet. $S_1$ is the state at which the first zero of the sequence has been detected. At $S_1$, if X=0 comes next, we can go back to $S_1$ since the last 0 is the start of a new sequence. IF X=1 happens, we move to $S_2$. At $S_2$, if X=0 happens, we move to $S_3$ and assert the output Z. if X=1 happens, we have generated the sequence 011 ($S_2$). This means we need to go back to $S_0$ and start all over again. At $S_3$, if 0 happens (010 ($S_3$) 0) it is the first digit of a new

sequence and we go to $S_1$. if $X=1$ happens ($\underbrace{0\,1\,0}_{S_3}\,1$), we go back to $S_0$ for a fresh start because the last $X=1$ does not mount to anything.

Notes:

1) In $S_0$, $S_1$ and $S_2$, we have $Z=0$ because the sequence has not been successfully completed. we do not write $Z=0$ next to these states but it is implied.

2) Transitions to different states can only happen with the clk (positive or negative edge of the clk) depending on which kind of Flip-flops are used to implement the machine.

3) In state $S_3$, when $X=1$ comes, one can take take the last two digits to be the state $S_2$ and make a transition to

$$\underbrace{0\,1\,0}_{S_3}\,\underbrace{1}_{S_2}$$

$S_2$ state. It is up to the designer's taste. At this point, we have drawn the state transition diagram. Next, we can draw the state transition table. Note that we have 4 states. One Flip-Flop can implement two states ($Q=0$, $Q=1$). Two Flip-flops can implement 4 states.

| $q_1$ | $q_2$ | state |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 1 | 3 |
| 1 | 0 | 4 |

4 states

Three Flip-Flops can implement eight states.

Here, we have Four states $S_0, S_1, S_2$ and $S_3$. We use Two Flip-Flops. we need to have state assignment. Let's use

| $q_A$ | $q_B$ | state assignment to binary code |
|---|---|---|
| 0 | 0 | $S_0$ |
| 0 | 1 | $S_1$ |
| 1 | 0 | $S_2$ |
| 1 | 1 | $S_3$ |

①

Any other assignment would work out too.

| $q_A$ | $q_B$ | |
|---|---|---|
| 0 | 0 | $S_1$ |
| 0 | 1 | $S_3$ |
| 1 | 0 | $S_0$ |
| 1 | 1 | $S_2$ |

②

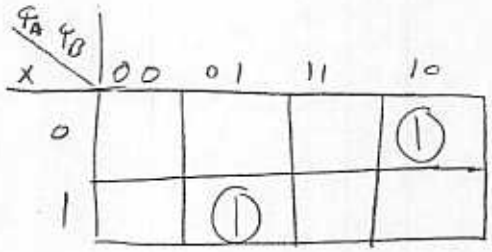
Let's choose assignment ①.

| Present state $q_A$ | $q_B$ | input $x$ | Next state $q_A$ | $q_B$ | output in present state $z$ | | $D_A$ | $D_B$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 ($S_0$) | 0 | 0 | 1 ($S_1$) | 0 | | 0 | 1 |
| 0 | 0 ($S_0$) | 1 | 0 | 0 ($S_0$) | 0 | | 0 | 0 |
| 0 | 1 ($S_1$) | 0 | 0 | 1 ($S_1$) | 0 | | 0 | 1 |
| 0 | 1 ($S_1$) | 1 | 1 | 0 ($S_2$) | 0 | | 1 | 0 |
| 1 | 0 ($S_2$) | 0 | 1 | 1 ($S_3$) | 0 | | 1 | 1 |
| 1 | 0 ($S_2$) | 1 | 0 | 0 ($S_0$) | 0 | | 0 | 0 |
| 1 | 1 ($S_3$) | 0 | 0 | 1 ($S_1$) | 1 | only in the present state of $S_3$, we have $z=1$ | 0 | 1 |
| 1 | 1 ($S_3$) | 1 | 0 | 0 ($S_0$) | 1 | | 0 | 0 |

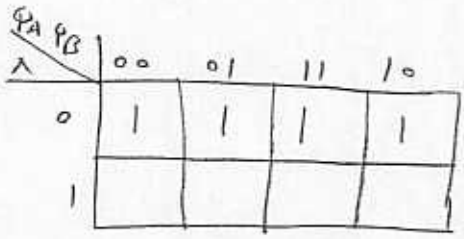
Let's suppose the two Flip-Flops we are going to use are D Flip-Flops. In the last column, we add the values of $D_A$ and $D_B$ required to take the machine From the $q_n$ (present) To $q_n$ (next state

and $Q_B$ (present) to $Q_B$ (next state). Note that $D_A = Q_A$ (next state) and $D_B = Q_B$ (next state) For D Flip-Flops.

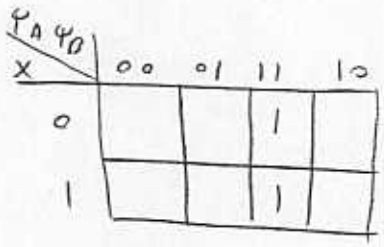
Now, we can Find $D_A$ and $D_B$ in terms of $Q_A$ (present state) and $Q_B$ (present state). we also Find Z.




$D_A = Q_A \bar{Q}_B \bar{X} + \bar{Q}_A Q_B X$

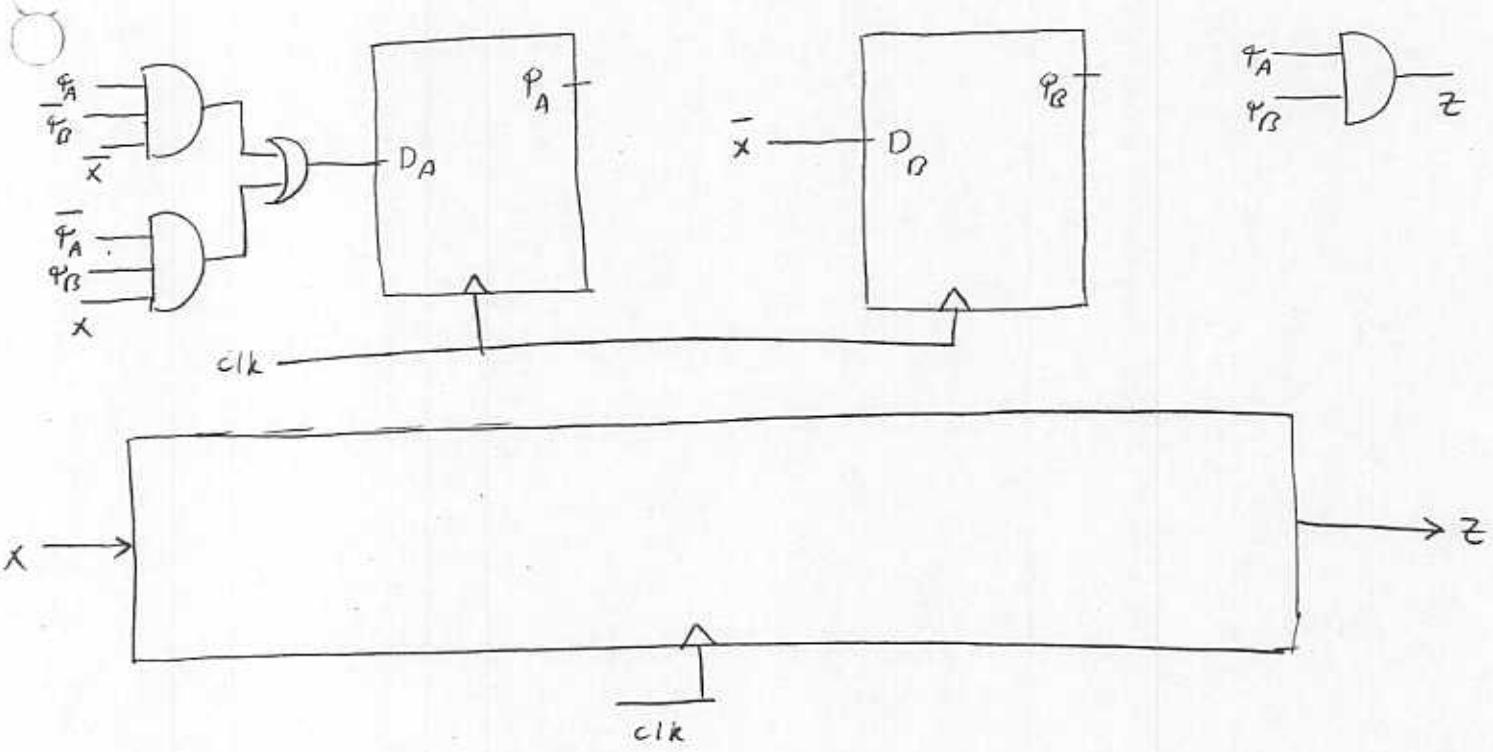



$D_B = \bar{X}$



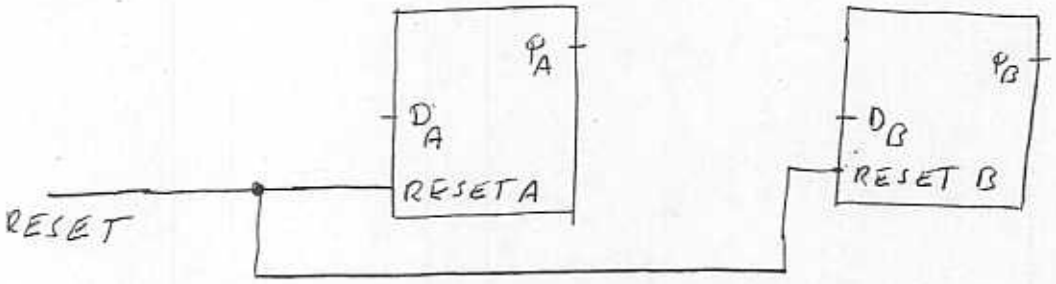

$Z = Q_A Q_B$

We can now draw the machine.




Note that the same clk runs both Flip-Flops. What about the RESET input we want to have to always go back to $S_0$ (00). Every Flip-Flop manufactured has an input called RESET.

When RESET is activated (RESET = logic 1 or 5V), it make Q of the Flip-Flop have a logic value of 0 regardless of the clk condition. RESET activated would make Q = 0 with no regard to the clk. ET is an asynchronous input. We can tie the RESETs of the two Flip-Flops together and call it the reset of the machine.




Same system RESET Feeds two input RESETs. When the master RESET is asserted, we will have $Q_A Q_B = 00 = S_0$. This takes the machine to the initial state right away which is what we want. Note that if we had used assignment #2, the machine would have ended up in state $S_1$ which is the first 0 detected. Assignment #2 can not implement master RESET using the RESET of every Flip-Flop.

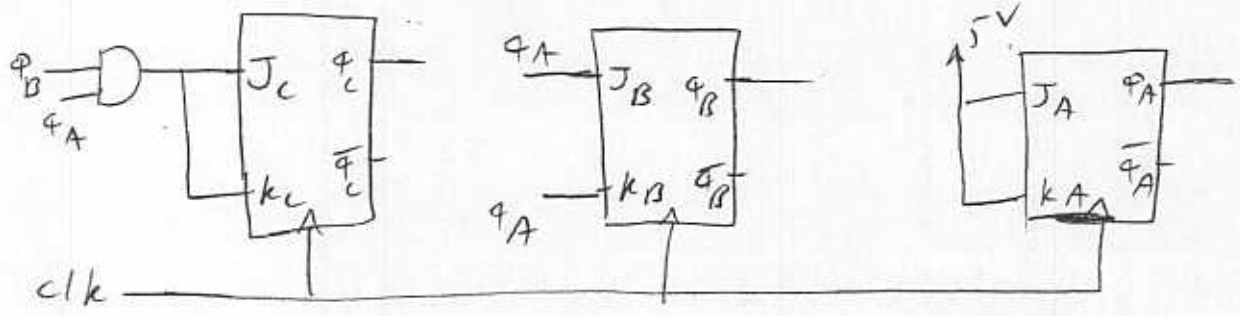
Note that starting from the design with D Flip-Flops you can now go backward to reach to the state transition table to verify that this machine does what it is supposed to do — detecting 010 sequence

ENGR. 2364
Handout #34

Analyzing sequential machines:

up to now, we have considered word problems that required a sequential machine for implementation. For instance, we designed a sequence detector by first trying its state transition diagram (STD). We then draw a state transition table (STT). We next draw k-maps for Js, ks or Ds and outputs in terms of present states and external inputs. Finally, we draw the circuit diagram. Now, we want to do exactly the opposite problem. Given a sequential circuit, analyze it to obtain the STD which tells you what the sequential machine is doing.

Ex. Analyze the sequential machine shown. Assume $q_C$, $q_B$ and $q_A$ are outputs.



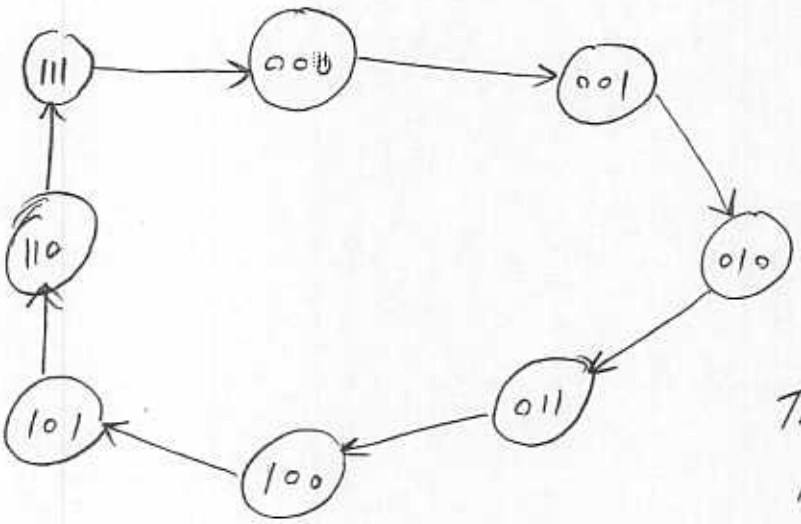
① Write down the expressions For $J_s$ and $k_s$ in terms of present state values.

$J_C = q_A q_B$, $K_C = q_A q_B$, $J_B = k_B = q_A$, $J_A = k_A = 1$

② Draw the STT

| Present state | | | | | | | | Next state | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $q_C$ | $q_B$ | $q_A$ | $J_C$ | $k_C$ | $J_B$ | $k_B$ | $J_A$ | $k_A$ | $q_C'$ | $q_B$ | $q_A$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

③ Draw STD

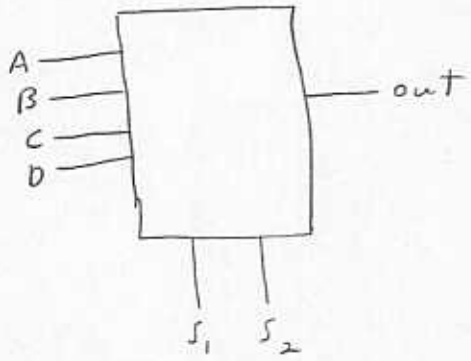



The circuit diagram is a 3-bit counter.

# Handout #34
# ENGR-364

## Four-input multiplexer:

Depending on the values of $S_1$ and $S_2$, one of the input lines is transmitted to the output.



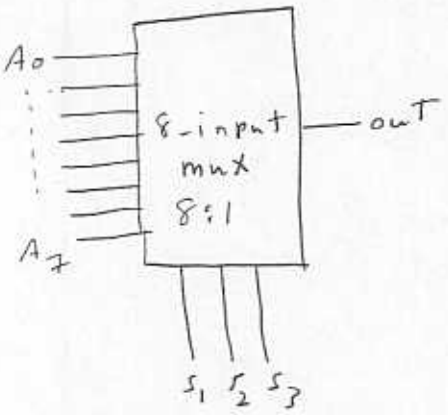

| $S_1$ | $S_2$ | out |
|---|---|---|
| 0 | 0 | A |
| 0 | 1 | B |
| 1 | 0 | C |
| 1 | 1 | D |

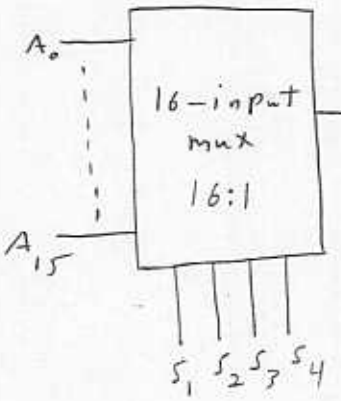
Without drawing a k-map, we can write

$out = \bar{S}_1 \bar{S}_2 A + \bar{S}_1 S_2 B + S_1 \bar{S}_2 C + S_1 S_2 D$, see last page for circuit diagram

Similarly, we can have eight-input and sixteen-input multiplexers.

Depending on which of the eight combinations of values $S_1 S_2 S_3$ take, one of the $A_0 - A_7$ is sent to the output.




Depending on which of the sixteen combinations of values $S_1 S_2 S_3 S_4$ take, one of $A_0 - A_{15}$ is sent to the output.

## Application of multiplexers:

① Implementing boolean Functions From truth table.

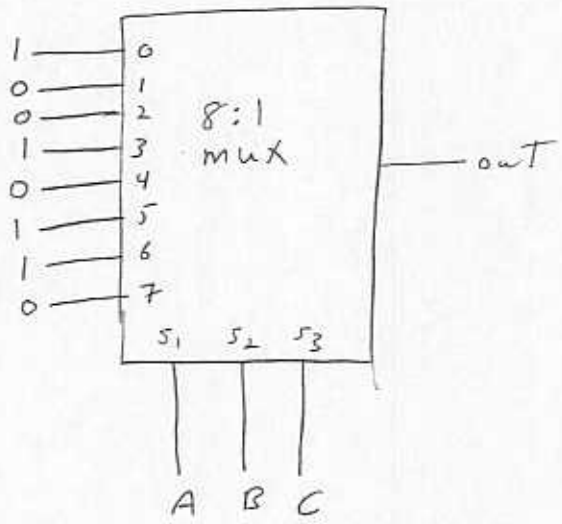
Consider the boolean Function shown below.

| decimal # | A | B | C | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 |

$F = \sum m(0, 3, 5, 6)$

This notation means that the Function F is 1 For any .F the minterms representing the decimal numbers 0, 3, 5 and 6.

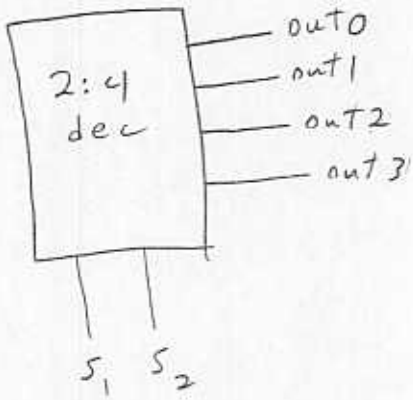
One way to implement F is to draw a k-map and use logic gates such as NOT, AND, OR, .... We can also implement F using 1 eight-input multiplexer.




Depending on what A, B and C take, the right input value is transmitted to the output.

2-input decoder or demultiplexer:

Depending on the values of $S_1$ and $S_2$, only one of the output lines become 1.



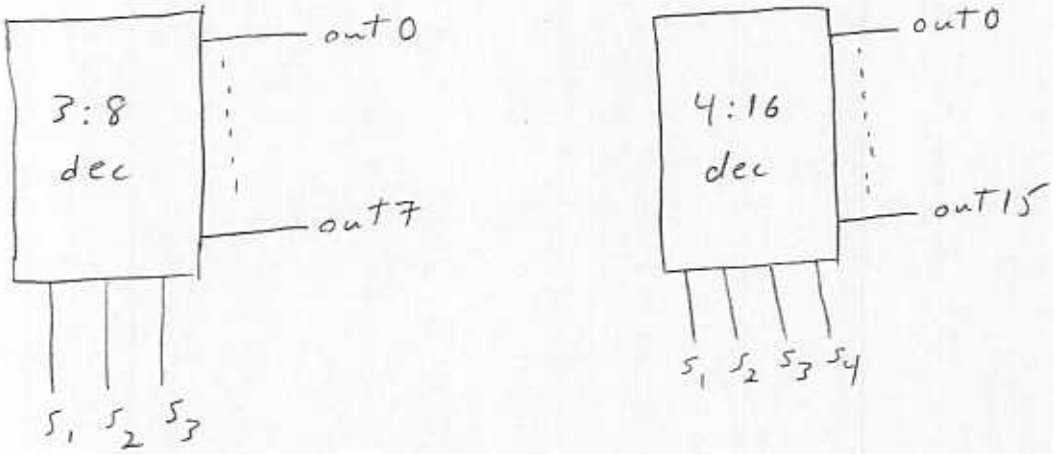

| $S_1$ | $S_2$ | out0 | out1 | out2 | out3 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

It is clear that $out0 = \overline{S_1}\,\overline{S_2}$, $out1 = \overline{S_1} S_2$, $out2 = S_1 \overline{S_2}$ and $out3 = S_1 S_2$.

Note that $S_1$ and $S_2$ are inputs and out1, out2, out3 and out4 are outputs.

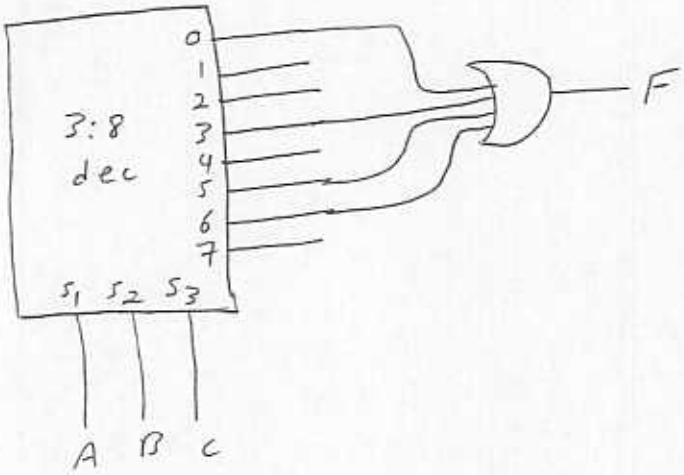
See last page for the circuit diagram

similarly, we can have 3:8 and 4:16 decoders.




Application of decoders:

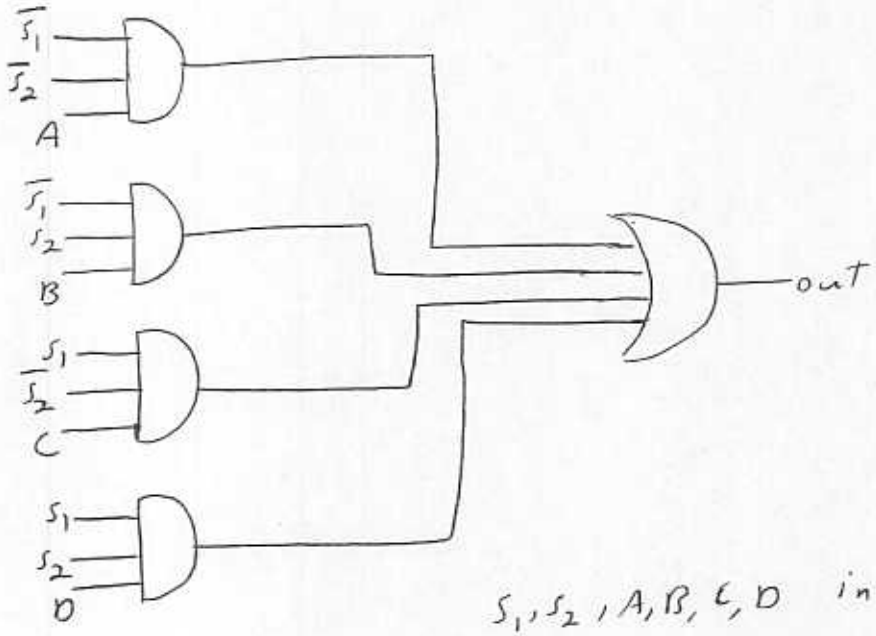
① Implementing boolean Functions from truth table.

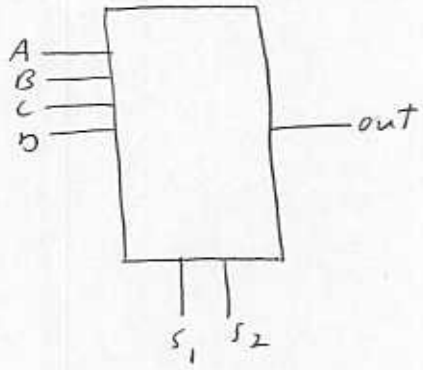



Note that depending on the combination of values of A, B and C, the output line that represents the decimal number of the ABC combination will go to 1. The four lines that implement minterms 0, 3, 5 and 6 are ORed together. If any of these four lines go to 1, F goes to 1.

# Handout #34
supplement
circuit diagrams

## 4:1 mux

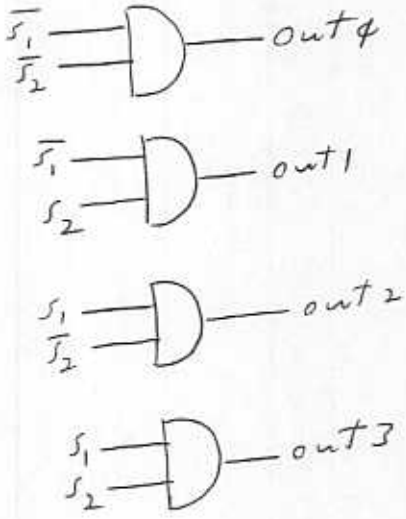


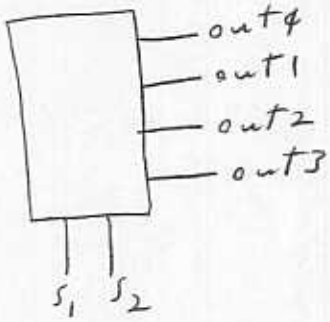




$S_1, S_2, A, B, C, D$ inputs

out output

## 2:4 decoder




$S_1, S_2$ input

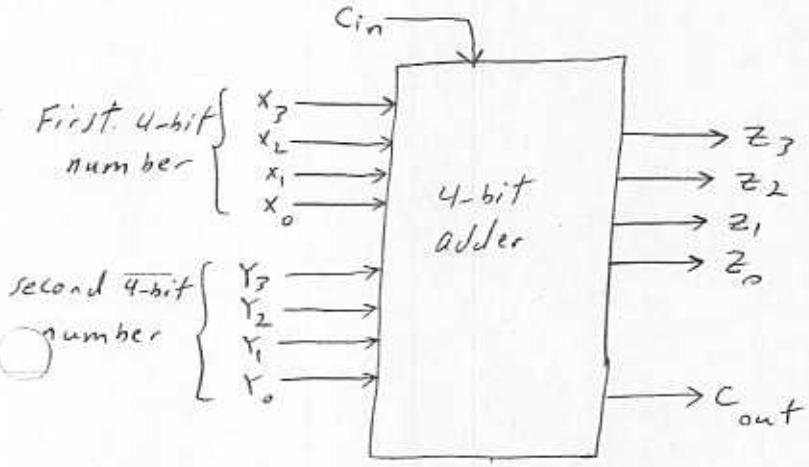
out0, out1, out2, out3 outputs

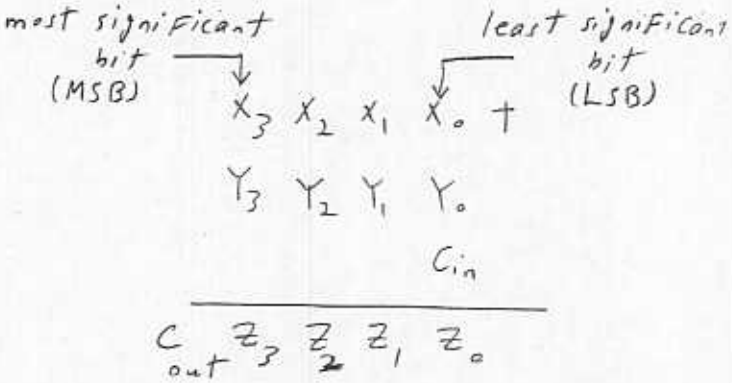
Binary addition:

| | | | | | |
|---|---|---|---|---|---|
| +3 | 0011 | +4 | 0100 | +2 | 0010 |
| +7 | 0111 | +8 | 1000 | +11 | 1011 |
| 10 | 1010 | 12 | 1100 | 13 | 1101 |

4-bit binary adder:

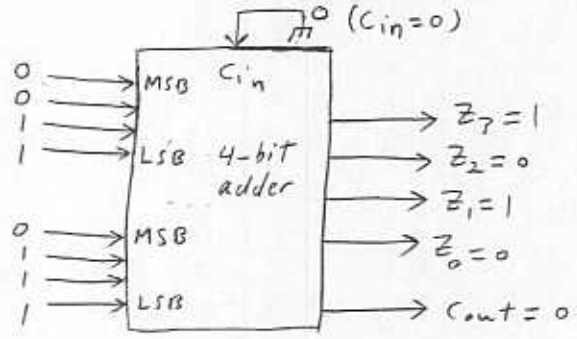
4-bit binary adders are used to add 4-bit numbers.




A 4-bit adder allowes for an addition bit ($C_{in}$ to be added to the two numbers.

Ex. Perform the first addition shown above with a Full adder.



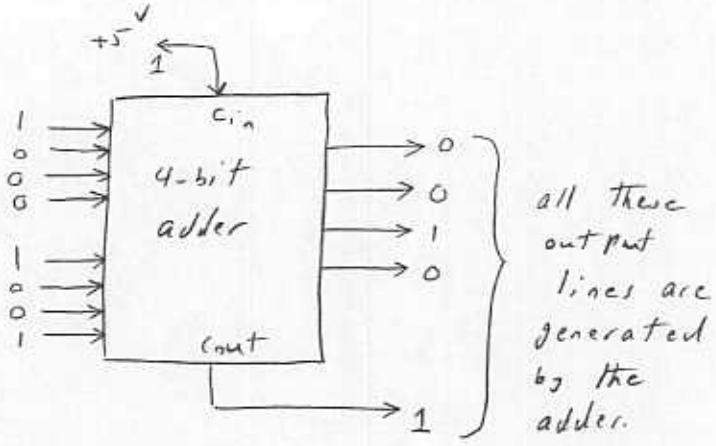

0011 +
0111
01010

These output lines are generated by the adder.

Ex. Perform the following addition using a 4-bit adder.

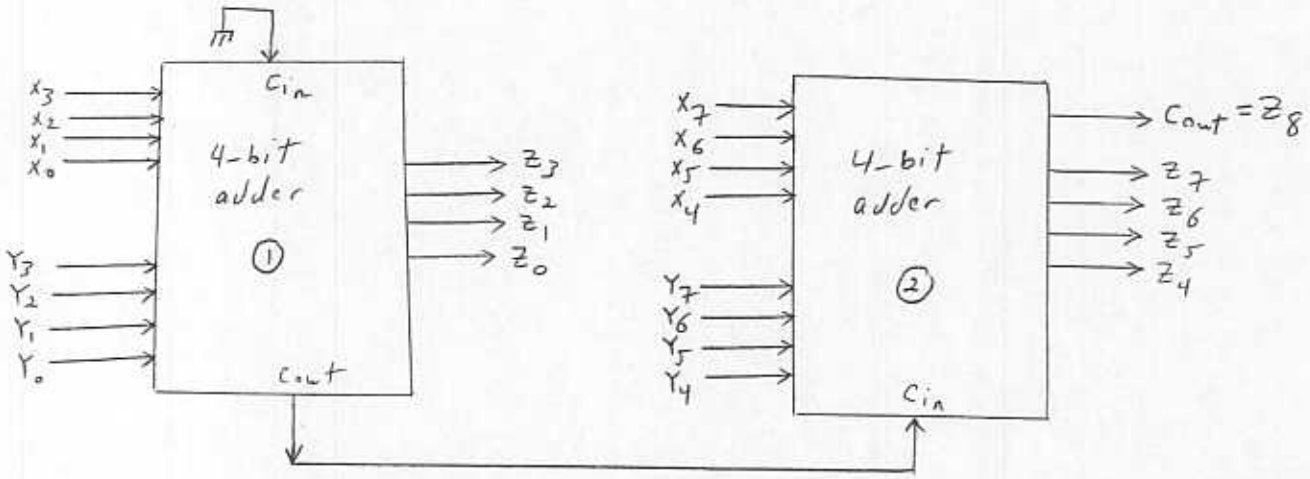
$$\begin{array}{r} +8 \\ +9 \\ C_{in} \rightarrow +\ 1 \\ \hline 18 \end{array} \qquad \begin{array}{r} 1000 \\ 1001 \\ \quad\ 1 \\ \hline 10010 \end{array}$$

$C_{out}$




Ex. Design an 8-bit adder using 4-bit adders.

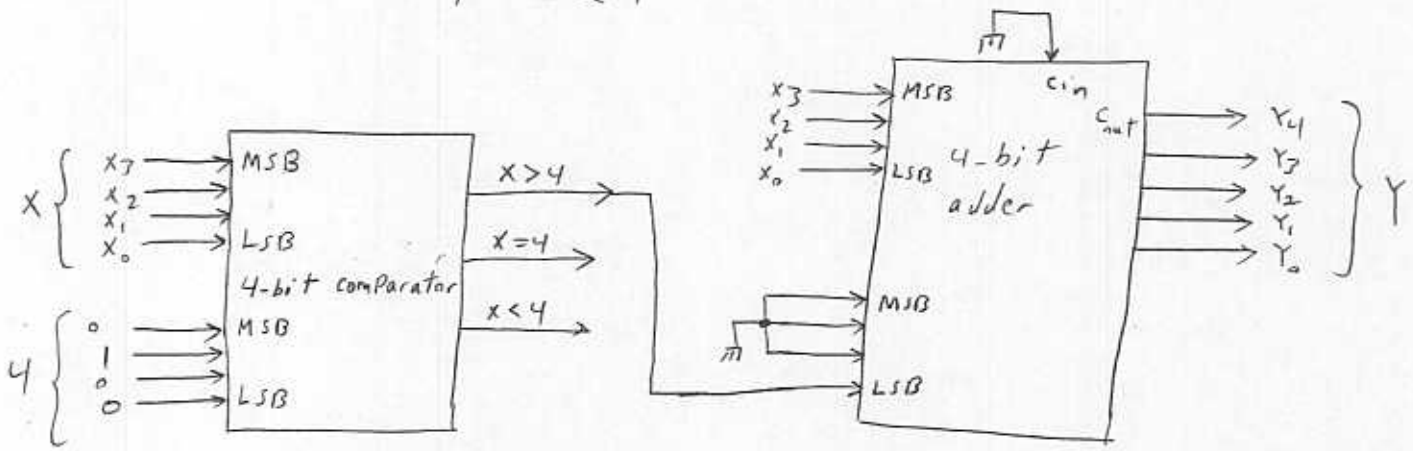
$$\begin{array}{r} X_7\ X_6\ X_5\ X_4\ X_3\ X_2\ X_1\ X_0 + \\ Y_7\ Y_6\ Y_5\ Y_4\ Y_3\ Y_2\ Y_1\ Y_0 \\ \hline Z_8\ Z_7\ Z_6\ Z_5\ Z_4\ Z_3\ Z_2\ Z_1\ Z_0 \end{array}$$




Note that for the first adder, $C_{in}$ is grounded (logic 0). Since there may be a carry out of adding the first four bits, this carry is taken to adder ② as $C_{in}$.

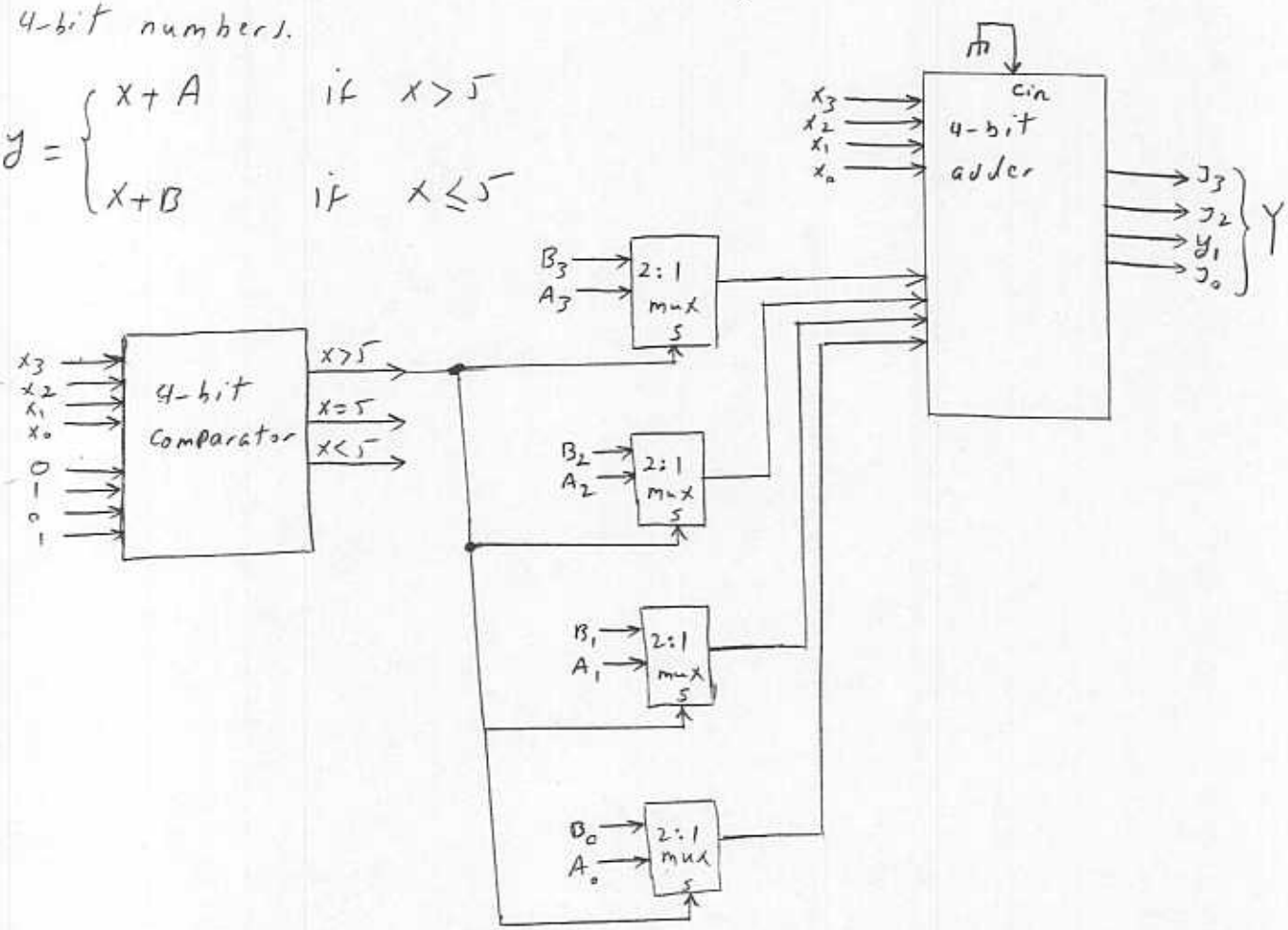
Ex. Design a circuit that implements $y$. $X$ is a 4-bit number.

$$y = \begin{cases} X+1 & \text{if } X > 4 \\ X & \text{if } X \leq 4 \end{cases}$$



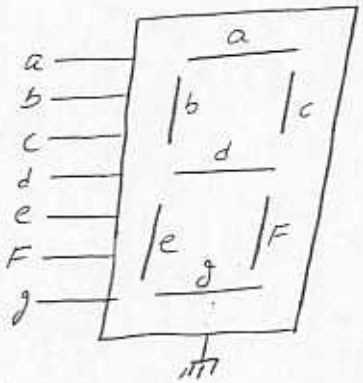

Ex. Design a circuit that implements $y$. $X$, $A$ and $B$ are all 4-bit numbers.

$$y = \begin{cases} X + A & \text{if } X > 5 \\ X + B & \text{if } X \leq 5 \end{cases}$$



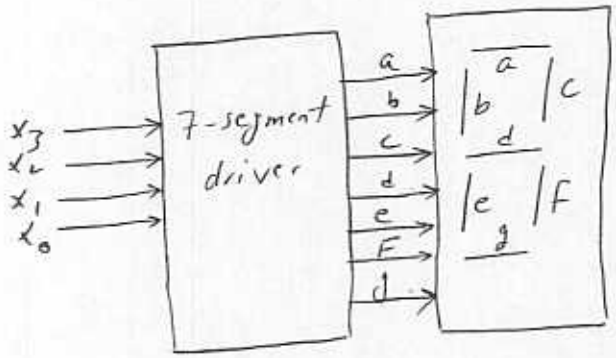
Note that if X is less than Five, then $\underline{X>5}$ line is a logic 0 and $B_3 B_2 B_1 B_0$ is passed to the adder. if X is greater than Five, then $\underline{X>5}$ line is a logic 1 and $A_3 A_2 A_1 A_0$ is passed to the adder.

Seven-segment display unit:



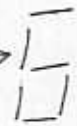

A seven-segment display unit has seven segments a, b, c, d, e, F and g that can turn on if the right input is at $5^V$ (logic 1) with respect to ground. For example, if you want to display 4, you need segments b, d, c and F to be at logic 1 and the rest logic 0.

Ex. Design a 7-segment display driver.




Anytime a binary number is presented at the input to the driver, the 7-segment display unit must display the number in decimal Form.

0110 ⟶

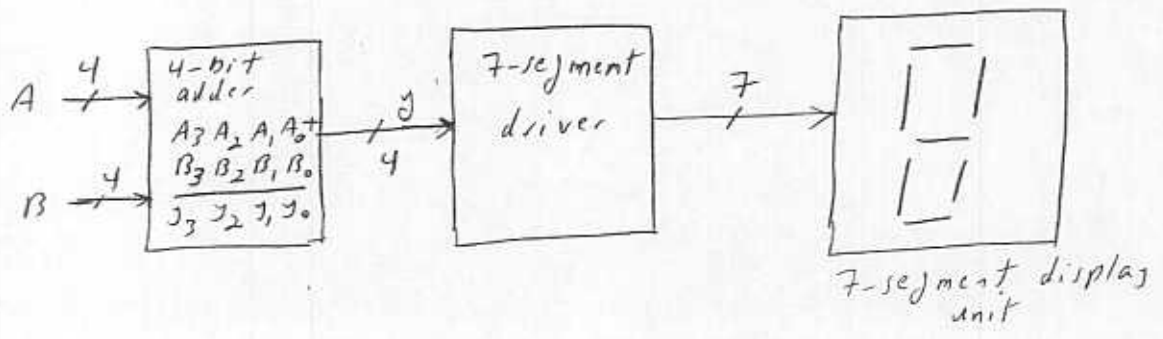


0101 ⟶

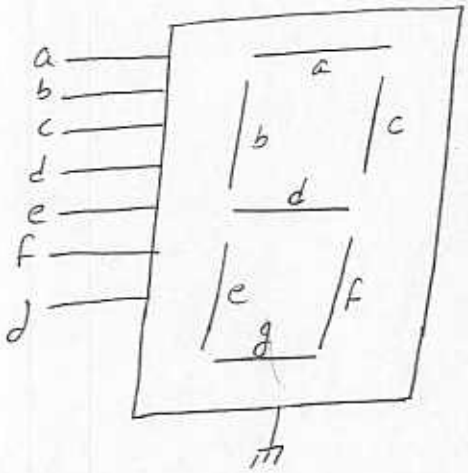
We start by drawing a truth table for the outputs a, b, c, d, e, f and g in terms of $X_3 X_2 X_1 X_0$.

| $X_3$ | $X_2$ | $X_1$ | $X_0$ | a | b | c | d | e | f | g | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | → 10 is assigned to the letter A |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | → 11 is assigned to the character ⊏ |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | → 12 is assigned to the character ⌊‾⌋ |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | → 13 " " " " " " ⌋ |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | → 14 " " " " " " ⌊ |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | → 15 " " " " " " ⌊‾⌋ |

Now, we can draw k-maps for all seven outputs which completes the design of the driver. 7-segment driver is a standard chip which is available for your usage. For example, the output of a 4-bit adder can be connected to a 7-segment driver and a 7-segment display unit to display the result of the addition



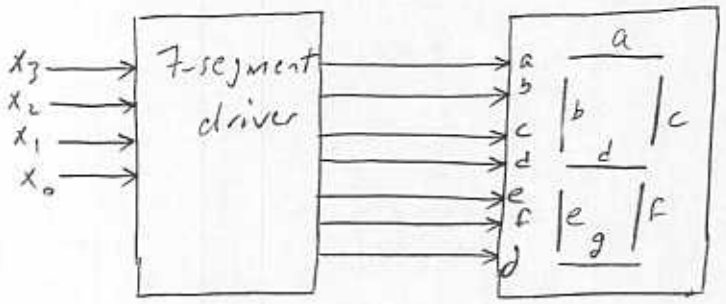
7-segment display unit:




By applying 5V or 0V (logic 1 or 0) to the seven inputs, the corresponding LED segment on the display will light up.

For example, to display 6 (six), apply a = b = d = e = f = g = 5V, c = 0.

There is another chip called a seven segment driver which is extremely useful.



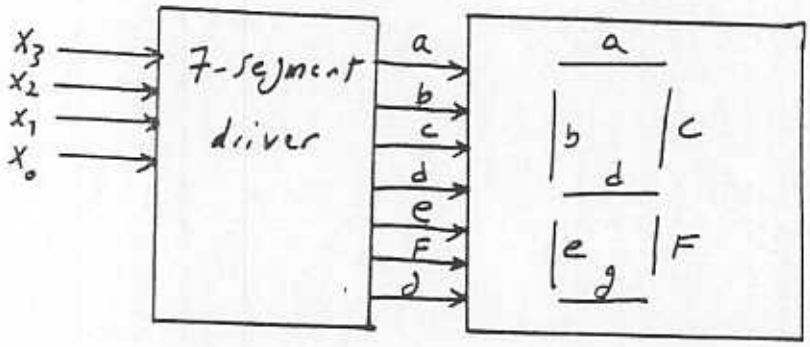

The 7-segment driver has 4 lines of input and seven lines of output to drive the display unit. the 7-segment driver is designed such that any binary number applied to it is displayed in decimal form on the display unit.

For example, if

$x_3 x_2 x_1 x_0 = 0110$, The display shows  $(a=b=d=e=g=f=1)$, $(c=0)$.

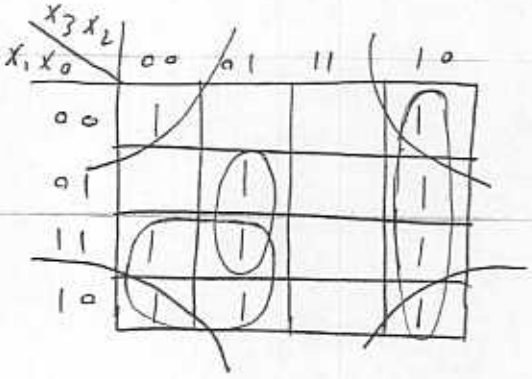
$x_3 x_2 x_1 x_0 = 0011$  $(a=c=d=f=g=1)$, $(b=e=0)$.

Let's design a 7-segment driver.



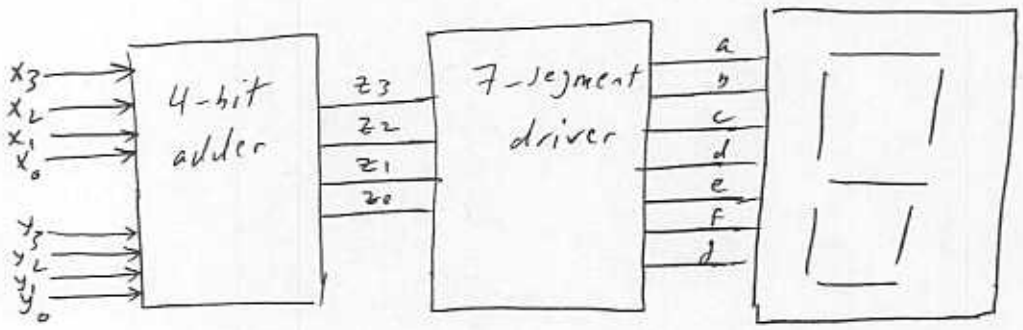

| $x_3$ | $x_2$ | $x_1$ | $x_0$ | a | b | c | d | e | f | g | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | → 10 is assigned to the letter A |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | → 11 is assigned to the character ‾\| |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | → 12 is assigned to the character \|_\| |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | → 13 " " " " " " \|‾ |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | → 14 " " " " " " \|_ |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | → 15 " " " " " " \|‾\| |

Now, Finish the design by drawing a k-map for outputs a, b, c, d, e, f, g in terms of $x_0$, $x_1$, $x_2$ and $x_3$. For example, the k-map for output a becomes:



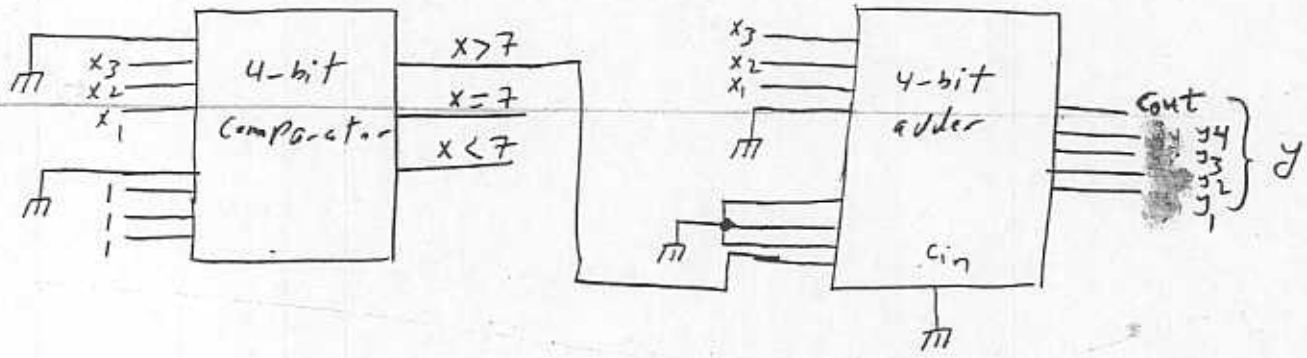

$$a = x_3 \bar{x}_2 + \bar{x}_3 x_1 + \bar{x}_2 \bar{x}_0 + \bar{x}_3 x_2 x_0$$

Now, we can design a circuit that would add two numbers and display the result. Suppose we want to add X ($x_3 x_2 x_1 x_0$) and Y ($y_3 y_2 y_1 y_0$) and display the result Z ($z_3 z_2 z_1 z_0$).



Ex. Design a circuit to perform the following function. X is a 3-bit number.

$$y = \begin{cases} 2x+1 & \text{if } x > 7 \\ 2x & \text{if } x \leq 7 \end{cases}$$




Note that the most significant bit of the 4-bit comparator that implements X is grounded. The number entered is $0x_3x_2x_1$ which is really $x_3x_2x_1$. To implement 2x, all we need to do is add a zero in front of $x_3x_2x_1$.

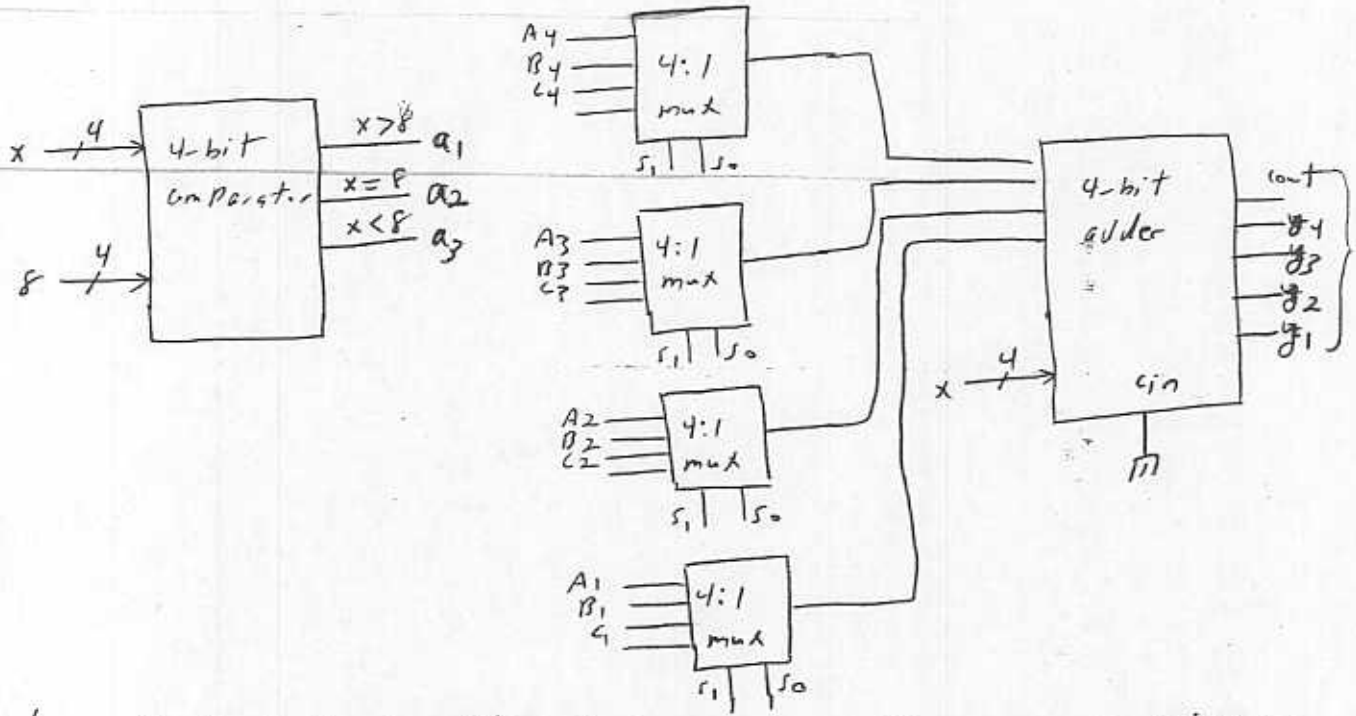
$$(X)_{10} = x_3x_2x_1 \Rightarrow (2x)_{10} = (x_3x_2x_10)_2$$

For instance, $(7)_{10} = (111)_2$, $(14)_{10} = (7x2)_{10} = (1110)_2$

The final output J may be 5 bits with Cout being the MSB.

Ex. Design a circuit to implement $y$. All variables are 4-bit numbers.

$$y = \begin{cases} x + A & \text{if } x < 8 \\ x + B & \text{if } x = 8 \\ x + C & \text{if } x > 8 \end{cases}$$




we need a truth table to determine $S_1$ and $S_0$ For every multiplexer in terms of the three output lines of the comparator.

| $a_1$ | $a_2$ | $a_3$ | $S_1$ | $S_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

Note that other combinations of $a_1, a_2$ and $a_3$ will not happen. Therefore, $S_1$ and $S_0$ can be don't cares.

| $a_3$ \ $a_1a_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | d | 0 | d | 1 |
| 1 | 0 | d | d | d |

$S_1 = a_1$

| $a_3$ \ $a_1a_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | d | 1 | d | 0 |
| 1 | 0 | d | d | d |

$S_0 = a_2$

Therefore, connect $a_1$ ($X > Y$ line) to $S_1$ and $a_2$ ($X = Y$ line) to $S_0$. Note that the Fourth input line of the multiplexer is not used and it will never transfer to the output. It is a good practice to connect this line to either $0^V$ or $5^V$. Input lines should not be left floating.