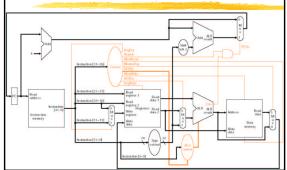
# Control and Multicycle Implementation

3-21-2003

### **Opening Discussion**

- What did we talk about last class?
- Have you seen anything interesting in the news? Will the Pentium M hit the desktop? What does that answer say about the hardware market?
- At least two people expressed confusion after last class. My first recommendation is to look at the figures in the book and try to trace out what each one does. Come to me if questions remain.

## **Datapath with Control Unit**



### **Single Cycle Control**

- Last time we saw the seven control lines that leave the control unit and direct the datapath.
  - RegDst tells if the write register destination is given by bits 20-16 in the instruction or 15-11
  - RegWrite if on we write a register value to memory.
  - ALUSrc tells us whether the second ALU operand is a register or the sign extended part of an instruction.

### **More Controls**

- The other 4.
  - PCSrc tells whether the new PC is coming from the ALU or a branch.
  - MemRead tells the memory to read from the incoming address.
  - MemWrite tells memory to write incoming value to income address.
  - MemtoReg tells whether register write data is from ALU or memory.

### **Adding Jumps**

To add jumps we put in just a few more pieces.

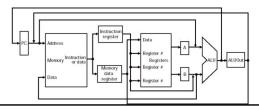


### Why Single Cycle Is Bad

- We want to go to a multicycle design for several reasons.
  - It gives us more speed because we don't have to have a clock cycle the length of the slowest instruction.
  - If they aren't all the same length we can optimize the common case.
  - We can't reuse functional units to it costs more to produce.

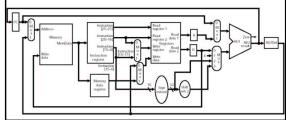
### **Multicycle Design**

We break each instruction into steps and the steps each take one cycle but a full instruction might take several cycles.



# Multicycle with Control Lines

Many control lines effectively tell us which step we are on.



# Complete Multicycle Datapath Transport of the Complete Multicycle Datap

### **Steps in Multicycle Path**

- Instruction fetch step
- Instruction decode and register fetch step
- Execution, memory address computation, or branch completion
- Memory access of R-type completion
- Memory read completion

### **Minute Essay**

- Can you think of any way that we might be able to do things better than the multicycle approach? In what way are we not fully utilizing the silicon on the chip?
- Next class we will continue to define the control of the multicycle approach and start talking about microprogramming.